Rabaey Digital Integrated Circuits Chapter 12

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology. Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible. The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design

hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

This volume describes the design of relay-based circuit systems from device fabrication to circuit micro-architectures. This book is ideal for both device engineers as well as circuit system designers, and highlights the importance of co-design across design hierarchies when trying to optimize system performance (in this case, energy-efficiency). The book will also appeal to researchers and engineers focused on semiconductor, integrated circuits, and energy efficient electronics.

Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the technology, circuit, logic and architectural levels, up to the system layer. The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction. Finally, it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments. The individual chapters are written by the leading researchers in the area, drawn from both industry and academia. Extensive references are included at the end of each chapter. Audience: A broad introduction for anyone interested in low power design. Can also be used as a text book for an advanced

graduate class. A starting point for any aspiring researcher.

In Thermal and Power Management of Integrated Circuits, power and thermal management issues in integrated circuits during normal operating conditions and stress operating conditions are addressed. Thermal management in VLSI circuits is becoming an integral part of the design, test, and manufacturing. Proper thermal management is the key to achieve high performance, quality and reliability. Performance and reliability of integrated circuits are strong functions of the junction temperature. A small increase in junction temperature may result in significant reduction in the device lifetime. This book reviews the significance of the junction temperature as a reliability measure under nominal and burn-in conditions. The latest research in the area of electro-thermal modeling of integrated circuits will also be presented. Recent models and associated CAD tools are covered and various techniques at the circuit and system levels are reviewed. Subsequently, the authors provide an insight into the concept of thermal runaway and how it may best be avoided. A section on low temperature operation of integrated circuits concludes the book.

This book will introduce new techniques for detecting and diagnosing small-delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small-delay defects, including important

parameters such as process variations, crosstalk, and power supply noise.

Regular Nanofabrics in Emerging Technologies gives a deep insight into both fabrication and design aspects of emerging semiconductor technologies, that represent potential candidates for the post-CMOS era. Its approach is unique, across different fields, and it offers a synergetic view for a public of different communities ranging from technologists, to circuit designers, and computer scientists. The book presents two technologies as potential candidates for future semiconductor devices and systems and it shows how fabrication issues can be addressed at the design level and vice versa. The reader either for academic or research purposes will find novel material that is explained carefully for both experts and non-initiated readers. Regular Nanofabrics in Emerging Technologies is a survey of post-CMOS technologies. It explains processing, circuit and system level design for people with various backgrounds.

Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets. Logical Effort: Designing Fast CMOS Circuits makes high speed design easier and more methodical, providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology, capacitance, and gate sizes. The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull, "logical effort" will change the way you approach design challenges. This book begins by equipping you with a sound understanding of the

method's essential procedures and concepts-so you can start using it immediately. Later chapters explore the theory and finer points of the method and detail its specialized applications. Features Explains the method and how to apply it in two practically focused chapters. Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions. Offers easy ways to choose the fastest circuit from among an array of potential circuit designs. Reduces the time spent on tweaking and simulations-so you can rapidly settle on a good design. Offers in-depth coverage of specialized areas of application for logical effort: skewed or unbalanced gates, other circuit families (including pseudo-NMOS and domino), wide structures such as decoders, and irregularly forking circuits. Presents a complete derivation of the method-so you see how and why it works.

A current trend in digital design-the integration of the MATLAB® components Simulink® and Stateflow® for model building, simulations, system testing, and fault detection-allows for better control over the design flow process and, ultimately, for better system results. Digital Integrated Circuits: Design-for-Test Using Simulink® and Stateflow® illustrates the construction of Simulink models for digital project test benches in certain design-for-test fields. The first two chapters of the book describe the major tools used for design-for-test. The author explains the process of Simulink model building, presents the main library blocks of Simulink, and examines the development of finite-state machine modeling using Stateflow diagrams. Subsequent

chapters provide examples of Simulink modeling and simulation for the latest design-for-test fields, including combinational and sequential circuits, controllability, and observability; deterministic algorithms; digital circuit dynamics; timing verification; built-in self-test (BIST) architecture; scan cell operations; and functional and diagnostic testing. The book also discusses the automatic test pattern generation (ATPG) process, the logical determinant theory, and joint test action group (JTAG) interface models. Digital Integrated Circuits explores the possibilities of MATLAB's tools in the development of application-specific integrated circuit (ASIC) design systems. The book shows how to incorporate Simulink and Stateflow into the process of modern digital design.

Modeling Microprocessor Performance focuses on the development of a design and evaluation tool, named RIPE (Rensselaer Interconnect Performance Estimator). This tool analyzes the impact on wireability, clock frequency, power dissipation, and the reliability of single chip CMOS microprocessors as a function of interconnect, device, circuit, design and architectural parameters. It can accurately predict the overall performance of existing microprocessor systems. For the three major microprocessor architectures, DEC, PowerPC and Intel, the results have shown agreement within 10% on key parameters. The models cover a broad range of issues that relate to the implementation and performance of single chip CMOS microprocessors. The book contains a detailed discussion of the various models and the underlying assumptions based on actual design practices. As such, RIPE and its models provide an insightful tool into single chip microprocessor design and its performance aspects. At the

same time, it provides design and process engineers with the capability to model, evaluate, compare and optimize single chip microprocessor systems using advanced technology and design techniques at an early design stage without costly and time consuming implementation. RIPE and its models demonstrate the factors which must be considered when estimating tradeoffs in device and interconnect technology and architecture design on microprocessor performance.

This book contains all the topics of importance to the low power designer. It first lays the foundation and then goes on to detail the design process. The book also discusses such special topics as power management and modal design, ultra low power, and low power design methodology and flows. In addition, coverage includes projections of the future and case studies.

This introductory book assumes minimal knowledge of the existence of integrated circuits and of the terminal behavior of electronic components such as resistors, diodes, and MOS and bipolar transistors. It presents to readers the basic information necessary for more advanced processing and design books. Focuses mainly on the basic processes used in fabrication, including lithography, oxidation, diffusion, ion implementation, and thin film deposition. Covers interconnection technology, packaging, and yield. Appropriate for readers interested in the area of fabrication of solid state devices and integrated circuits.

Introduction to Electronics/ Microelectronics at Junior Level. This text describes device physics and circuit design in the context of modern microelectronics integrated circuit technology. It introduces approaches to learning the core device physics and analog/digital circuit concepts that make the subject more accessible to the current generation of students. The authors have designed a concise, concentrated presentation, limiting coverage to only those concepts

necessary for the understanding of devices and circuits. Beginning with discussions on the operation of electronic devices and analysis of the nucleus of digital design, the text addresses: the impact of interconnect, design for low power, issues in timing and clocking, design methodologies, and the effect of design automation on the digital design perspective.
This monograph is motivated by the challenges faced in designing reliable VLSI systems in modern VLSI processes. The reliable operation of integrated circuits (ICs) has become increasingly dif?cult to achieve in the deep submicron (DSM) era. With continuouslydecreasing device feature sizes, combinedwith lower supply voltages and higher operating frequencies, the noise immunity of VLSI circuits is decreasing alarmingly. Thus, VLSI circuits are becoming more vulnerable to noise effects such as crosstalk, power supply variations, and radiation-inducedsoft errors. Among these noise sources, soft errors(or error caused by radiation particle strikes) have become an increasingly troublesome issue for memory arrays as well as c- binational logic circuits. Also, in the DSM era, process variations are increasing at a signi?cant rate, making it more dif?cult to design reliable VLSI circuits. Hence, it is important to ef?ciently design robust VLSI circuits that are resilient to radiation particle strikes and process variations. The work presented in this research mo- graph presents several analysis and design techniques with the goal of realizing VLSI circuits, which are radiation and process variation tolerant.
The 2nd Edition of Analog Integrated Circuit Design focuses on more coverage about several types of circuits that have increased in importance in the past decade. Furthermore, the text is enhanced with material on CMOS IC device modeling, updated processing layout and expanded coverage to reflect technical innovations. CMOS devices and circuits have more influence in this edition as well as a reduced amount of text

on BiCMOS and bipolar information. New chapters include topics on frequency response of analog ICs and basic theory of feedback amplifiers.

As advances in technology and circuit design boost operating frequencies of microprocessors, DSPs and other fast chips, new design challenges continue to emerge. One of the major performance limitations in today's chip designs is clock skew, the uncertainty in arrival times between a pair of clocks. Increasing clock frequencies are forcing many engineers to rethink their timing budgets and to use skew-tolerant circuit techniques for both domino and static circuits. While senior designers have long developed their own techniques for reducing the sequencing overhead of domino circuits, this knowledge has routinely been protected as trade secret and has rarely been shared. Skew-Tolerant Circuit Design presents a systematic way of achieving the same goal and puts it in the hands of all designers. This book clearly presents skew-tolerant techniques and shows how they address the challenges of clocking, latching, and clock skew. It provides the practicing circuit designer with a clearly detailed tutorial and an insightful summary of the most recent literature on these critical clock skew issues. * Synthesizes the most recent advances in skew-tolerant design in one cohesive tutorial * Provides incisive instruction and advice punctuated by humorous illustrations * Includes exercises to test understanding of key concepts and solutions to selected exercises

Intended for use in undergraduate senior-level digital circuit design courses with advanced material sufficient for graduate-level courses. Progressive in content and form, this text successfully bridges the gap between the circuit perspective and system perspective of digital integrated circuit design. Beginning with solid discussions on the operation of electronic devices and in-depth analysis of the nucleus of

digital design, the text maintains a consistent, logical flow of subject matter throughout. The revision addresses today's most significant and compelling industry topics, including: the impact of interconnect, design for low power, issues in timing and clocking, design methodologies, and the tremendous effect of design automation on the digital design perspective. The revision reflects the ongoing evolution in digital integrated circuit design, especially with respect to the impact of moving into the deep-submicron realm.

Until the 1990s, the reduction of the minimum feature sizes used to fabricate in- grated circuits, called “scaling”, has highlighted serious advantages as integration density, speed, power consumption, functionality and cost. Direct consequence was the decrease of cost-per-function, so the electronic productivity has largely progressed in this period. Another usually cited trend is the evolution of the in- gration density as expressed by the well-know Moore’s Law in 1975: the number of devices per chip doubles every 2 years. This evolution has allowed improving signi?cantly the circuit complexity, offering a great computing power in the case of microprocessor, for example. However, since few years, signi?cant issues appeared such as the increase of the circuit heating, device complexity, variability and dif?culties to improve the integration density. These new trends generate an important growth in development and production costs. Though is it, since 40 years, the evolution of the microelectronics always f- lowed the Moore’s law and each dif?culty has found a solution.

Digital Integrated CircuitsA Design Perspective

For Electrical Engineering and Computer Engineering courses that cover the design and technology of very large scale integrated (VLSI) circuits and systems. May also be used as a VLSI reference for professional VLSI design engineers, VLSI design managers, and VLSI CAD engineers.

Modern VSLI Design provides a comprehensive “bottom-up” guide to the design of VSLI systems, from the physical design of circuits through system architecture with focus on the latest solution for system-on-chip (SOC) design. Because VSLI system designers face a variety of challenges that include high performance, interconnect delays, low power, low cost, and fast design turnaround time, successful designers must understand the entire design process. The Third Edition also provides a much more thorough discussion of hardware description languages, with introduction to both Verilog and VHDL. For that reason, this book presents the entire VSLI design process in a single volume.

For upper level and graduate level Electrical and Computer Engineering courses in Integrated Circuit Design as well as professional circuit designers, engineers and researchers working in portable wireless communications hardware. This book presents the fundamentals of Complementary Metal Oxide Semiconductor (CMOS) and Bipolar compatible Complementary Metal Oxide Semiconductor (BiCMOS) technology, as well as the latest technological advances in the field. It discusses the concepts and techniques of new integrated circuit design for building high performance and low power circuits and systems for current and future very-large-scale-integration (VLSI) and giga-scale-integration (GSI) applications. CMOS/BiCMOS ULSI: Low-Voltage Low-Power is an essential resource for every professional moving toward lower voltage, lower power, and higher performance VLSI circuits and subsystems design.

For the new millenium, Wai-Kai Chen introduced a monumental reference for the design, analysis, and prediction of VLSI circuits: The VLSI Handbook. Still a valuable tool for dealing with the most dynamic field in engineering, this second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts, models, and

equations. Written by a stellar international panel of expert contributors, this handbook is a reliable, comprehensive resource for real answers to practical problems. It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus. WHAT'S IN THE SECOND EDITION? Sections on... Low-power electronics and design VLSI signal processing Chapters on... CMOS fabrication Content-addressable memory Compound semiconductor RF circuits High-speed circuit design principles SiGe HBT technology Bipolar junction transistor amplifiers Performance modeling and analysis using SystemC Design languages, expanded from two chapters to twelve Testing of digital systems Structured for convenient navigation and loaded with practical solutions, The VLSI Handbook, Second Edition remains the first choice for answers to the problems and challenges faced daily in engineering practice.

This book teaches the principles of physical design, layout, and simulation of CMOS integrated circuits. It is written around a very powerful CAD program called Microwind that is available on the accompanying CD-ROM. Featuring a friendly interface, Microwind is both educational and useful for designing CMOS chips.

The fourth edition of CMOS Digital Integrated Circuits: Analysis and Design continues the well-established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design, as well as addressing state-of-the-art technology issues highlighted by the widespread use of nanometer-scale CMOS technologies. In this latest edition, virtually all chapters have been re-written, the transistor model equations and device parameters have been revised to reflect the sigificant changes that must be taken into account for new technology generations, and the material has been reinforced with up-to-date examples.

The broad-ranging coverage of this textbook starts with the fundamentals of CMOS process technology, and continues with MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, arithmetic building blocks, clock and I/O circuits, low power design techniques, design for manufacturability and design for testability.

This book pioneers the field of gain-cell embedded DRAM (GC-eDRAM) design for low-power VLSI systems-on-chip (SoCs). Novel GC-eDRAMs are specifically designed and optimized for a range of low-power VLSI SoCs, ranging from ultra-low power to power-aware high-performance applications. After a detailed review of prior-art GC-eDRAMs, an analytical retention time distribution model is introduced and validated by silicon measurements, which is key for low-power GC-eDRAM design. The book then investigates supply voltage scaling and near-threshold voltage (NTV) operation of a conventional gain cell (GC), before presenting novel GC circuit and assist techniques for NTV operation, including a 3-transistor full transmission-gate write port, reverse body biasing (RBB), and a replica technique for optimum refresh timing. Next, conventional GC bitcells are evaluated under aggressive technology and voltage scaling (down to the subthreshold domain), before novel bitcells for aggressively scaled CMOS nodes and soft-error tolerance as presented, including a 4-transistor GC with partial internal feedback and a 4-transistor GC with built-in redundancy.

The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

This textbook for a one-semester course in Digital Systems Design describes the basic methods used to develop “traditional” Digital Systems, based on

the use of logic gates and flip flops, as well as more advanced techniques that enable the design of very large circuits, based on Hardware Description Languages and Synthesis tools. It was originally designed to accompany a MOOC (Massive Open Online Course) created at the Autonomous University of Barcelona (UAB), currently available on the Coursera platform. Readers will learn what a digital system is and how it can be developed, preparing them for steps toward other technical disciplines, such as Computer Architecture, Robotics, Bionics, Avionics and others. In particular, students will learn to design digital systems of medium complexity, describe digital systems using high level hardware description languages, and understand the operation of computers at their most basic level. All concepts introduced are reinforced by plentiful illustrations, examples, exercises, and applications. For example, as an applied example of the design techniques presented, the authors demonstrate the synthesis of a simple processor, leaving the student in a position to enter the world of Computer Architecture and Embedded Systems. Wafer-level testing refers to a critical process of subjecting integrated circuits and semiconductor devices to electrical testing while they are still in wafer form. Burn-in is a temperature/bias reliability stress test used in detecting and screening out potential early life device failures. This hands-on

resource provides a comprehensive analysis of these methods, showing how wafer-level testing during burn-in (WLTBI) helps lower product cost in semiconductor manufacturing. Engineers learn how to implement the testing of integrated circuits at the wafer-level under various resource constraints. Moreover, this unique book helps practitioners address the issue of enabling next generation products with previous generation testers. Practitioners also find expert insights on current industry trends in WLTBI test solutions.

In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should also be

used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications.
KEY BENEFIT: This hands-on book leads readers through the complete process of building a ready-to-fabricate CMOS integrated circuit using popular commercial design software. KEY TOPICS: The VLSI CAD flow described in this book uses tools from two vendors: Cadence Design Systems, Inc. and Synopsys Inc. Detailed tutorials include step-by-step instructions and screen shots of tool windows and dialog boxes. MARKET: A useful reference for chip designers.

The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, Low-Power CMOS Circuits: Technology,

Logic Design, and CAD Tools addresses the design of low-power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low-power circuitry, from transistors to logic gates. The book is organized into three broad sections for convenient access. The first examines the history of low-power electronics along with a look at emerging and possible future technologies. It also considers other technologies, such as nanotechnologies and optical chips, that may be useful in designing integrated circuits. The second part explains the techniques used to reduce power consumption at low levels. These include clock gating, leakage reduction, interconnecting and communication on chips, and adiabatic circuits. The final section discusses various CAD tools for designing low-power circuits. This section includes three chapters that demonstrate the tools and low-power design issues at three major companies that produce logic synthesizers. Providing detailed examinations contributed by leading experts, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits. It is a must-read for anyone designing modern computers or embedded systems.

This book focuses on increasing the energy-efficiency of electronic devices so that portable

applications can have a longer stand-alone time on the same battery. The authors explain the energy-efficiency benefits that ultra-low-voltage circuits provide and provide answers to tackle the challenges which ultra-low-voltage operation poses. An innovative design methodology is presented, verified, and validated by four prototypes in advanced CMOS technologies. These prototypes are shown to achieve high energy-efficiency through their successful functionality at ultra-low supply voltages.

This book provides a single-source reference to the state-of-the-art of high-level programming models and compilation tool-chains for embedded system platforms. The authors address challenges faced by programmers developing software to implement parallel applications in embedded systems, where very often they are forced to rewrite sequential programs into parallel software, taking into account all the low level features and peculiarities of the underlying platforms. Readers will benefit from these authors' approach, which takes into account both the application requirements and the platform specificities of various embedded systems from different industries. Parallel programming tool-chains are described that take as input parameters both the application and the platform model, then determine relevant transformations and mapping decisions on the concrete platform, minimizing user intervention and hiding the difficulties related to the correct and efficient use of memory hierarchy and low level code generation.

In response to tremendous growth and new technologies in the semiconductor industry, this volume is organized into five, information-rich sections. Digital Design and Fabrication

surveys the latest advances in computer architecture and design as well as the technologies used to manufacture and test them. Featuring contributions from leading experts, the book also includes a new section on memory and storage in addition to a new chapter on nonvolatile memory technologies. Developing advanced concepts, this sharply focused book— Describes new technologies that have become driving factors for the electronic industry Includes new information on semiconductor memory circuits, whose development best illustrates the phenomenal progress encountered by the fabrication and technology sector Contains a section dedicated to issues related to system power consumption Describes reliability and testability of computer systems Pinpoints trends and state-of-the-art advances in fabrication and CMOS technologies Describes performance evaluation measures, which are the bottom line from the user's point of view Discusses design techniques used to create modern computer systems, including high-speed computer arithmetic and high-frequency design, timing and clocking, and PLL and DLL design

Design and Analysis of High Efficiency Line Drivers for xDSL covers the most important building block of an xDSL (ADSL, VDSL, ...) system: the line driver. Traditional Class AB line drivers consume more than 70% of the total power budget of state-of-the-art ADSL modems. This book describes the main difficulties in designing line drivers for xDSL. The most important specifications are elaborated staring from the main properties of the channel and the signal properties. The traditional (class AB), state-of-the-art (class G) and future technologies (class K) are discussed. The main part of Design and Analysis of High Efficiency Line Drivers for xDSL describes the design of a novel architecture: the Self-Oscillating Power Amplifier or SOPA.

Written by the world's most prominent microprocessor design

leaders from industry and academia, this book provides complete coverage of all aspects of complex microprocessor design: technology, power management, clocking, high-performance architecture, design methodologies, memory and I/O design, computer aided design, testing and design for testability. The chapters provide state-of-the-art knowledge while including sufficient tutorial material to bring non-experts up to speed. A useful companion to design engineers working in related areas.

Copyright: 35866d4c6fea5f83a41fc40df1c4db5d