High Speed Serdes Devices And Applications

This book discusses the latest developments and outlines future trends in the fields of microelectronics, electromagnetics and telecommunication. It includes original research presented at the International Conference on Microelectronics, Electromagnetics and Telecommunication (ICMEET 2019), organized by the Department of ECE, Raghu Institute of Technology, Andhra Pradesh, India. Written by scientists, research scholars and practitioners from leading universities, engineering colleges and R&D institutes around the globe, the papers share the latest breakthroughs in and promising solutions to the most important issues facing today's society.

This book provides a thorough overview of cutting-edge research on electronics applications relevant to industry, the environment, and society at large. It covers a broad spectrum of application domains, from automotive to space and from health to security, while devoting special attention to the use of embedded devices and sensors for imaging, communication and control. The book is based on the 2020 ApplePies Conference, held online in November 2020, which brought together researchers and stakeholders to consider the most significant current trends in the field of applied electronics and to debate visions for the

future. Areas addressed by the conference included information communication technology; biotechnology and biomedical imaging; space; secure, clean and efficient energy; the environment; and smart, green and integrated transport. As electronics technology continues to develop apace, constantly meeting previously unthinkable targets, further attention needs to be directed toward the electronics applications and the development of systems that facilitate human activities. This book, written by industrial and academic professionals, represents a valuable contribution in this endeavor.

This book describes the most frequently used high-speed serial buses in embedded systems, especially those used by FPGAs. These buses employ SerDes, JESD204, SRIO, PCIE, Aurora and SATA protocols for chip-to-chip and board-to-board communication, and CPCIE, VPX, FC and Infiniband protocols for inter-chassis communication. For each type, the book provides the bus history and version info, while also assessing its advantages and limitations. Furthermore, it offers a detailed guide to implementing these buses in FPGA design, from the physical layer and link synchronization to the frame format and application command. Given its scope, the book offers a valuable resource for researchers, R&D engineers and graduate students in computer science or electronics who wish to learn the protocol principles, structures and applications

of high-speed serial buses.

Master the usage of s-parameters in signal integrity applications and gain full understanding of your simulation and measurement environment with this rigorous and practical guide. Solve specific signal integrity problems including calculation of the s-parameters of a network, linear simulation of circuits, de-embedding, and virtual probing, all with expert guidance. Learn about the interconnectedness of s-parameters, frequency responses, filters, and waveforms. This invaluable resource for signal integrity engineers is supplemented with the open-source software SignalIntegrity, a Python package for scripting solutions to signal integrity problems.

This book is based on the class notes of a VLSI design course the author offered in Electrical Engineering Department at Arizona State University. The materials are organized into twenty-one special topics covering various aspects of analysis, modeling, and implementation of VLSI high-speed I/O circuits, such as prototype timing models, jitter analysis, transmitter, receiver, equalizer, phase-locked loop (PLL), and data recovery circuit designs.

This book introduces a wide range of existing and potential applications for asynchronous circuits, each accompanied with the corresponding circuit design theory, sample circuit implementations, results, and analysis.

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular

Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

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Analog Circuit Design is based on the yearly Advances in Analog Circuit Design workshop. The aim of the workshop is to bring together designers of advanced analogue and RF circuits for the purpose of studying and discussing new possibilities and future developments in this field. Selected topics for AACD 2007 were: (1) Sensors, Actuators and Power Drivers for the Automotive and Industrial Environment; (2) Integrated PA's from Wireline to RF; (3) Very High Frequency Front Ends.

This book describes for readers the entire, interconnected complex of theoretical and practical aspects of designing and organizing the production of various electronic devices, the general and main distinguishing feature of which is the high speed of processing and transmitting of digital signals. The authors discuss all the main stages of design - from the upper system level of the hierarchy (telecommunications system, 5G mobile communications) to the lower level of basic semiconductor elements, printed circuit boards. Since the developers of these devices in practice deal with distorted digital signals that are transmitted against a background of interference, the authors not only explain the physical nature of such effects, but also offer specific solutions as to how to avoid such parasitic effects, even at the design stage of high-speed devices.

This book provides comprehensive coverage of the dependability challenges in today's advanced computing systems. It is an in-depth discussion of all the technological and design-

level techniques that may be used to overcome these issues and analyzes various dependability-assessment methods. The impact of individual application scenarios on the definition of challenges and solutions is considered so that the designer can clearly assess the problems and adjust the solution based on the specifications in question. The book is composed of three sections, beginning with an introduction to current dependability challenges arising in complex computing systems implemented with nanoscale technologies, and of the effect of the application scenario. The second section details all the fault-tolerance techniques that are applicable in the manufacture of reliable advanced computing devices. Different levels, from technology-level fault avoidance to the use of error correcting codes and system-level checkpointing are introduced and explained as applicable to the different application scenario requirements. Finally the third section proposes a roadmap of future trends in and perspectives on the dependability and manufacturability of advanced computing systems from the special point of view of industrial stakeholders. Dependable Multicore Architectures at Nanoscale showcases the original ideas and concepts introduced into the field of nanoscale manufacturing and systems reliability over nearly four years of work within COST Action IC1103 MEDIAN, a think-tank with participants from 27 countries. Academic researchers and graduate students working in multi-core computer systems and their manufacture will find this book of interest as will industrial design and manufacturing engineers working in VLSI companies.

This book is a step-by-step tutorial on how to design a low-power, high-resolution (not less than 12 bit), and high-speed (not less than 200 MSps) integrated CMOS analog-to-digital (AD) converter, to respond to the challenge from the rapid growth of IoT. The discussion includes

design techniques on both the system level and the circuit block level. In the architecture level, the power-efficient pipelined AD converter, the hybrid AD converter and the time-interleaved AD converter are described. In the circuit block level, the reference voltage buffer, the opamp, the comparator, and the calibration are presented. Readers designing low-power and high-performance AD converters won't want to miss this invaluable reference. Provides an in-depth introduction to the newest design techniques for the power-efficient, high-resolution (not less than 12 bit), and high-speed (not less than 200 MSps) AD converter; Presents three types of power-efficient architectures of the high-resolution and high-speed AD converter; Discusses the relevant circuit blocks (i.e., the reference voltage buffer, the opamp, and the comparator) in two aspects, relaxing the requirements and improving the performance.

This book presents the necessary concepts for the design and testing of radiofrequency and high-speed circuits. Signal and propagation theory is presented for the various circuit levels, from the chip to the PCB. The co-existence of high-speed wideband signals of radiofrequency signals and supply circuits is developed in order to provide design rules for engineers and Masters-level students. The subjects covered include: interconnections and signal integrity; spectral analysis techniques for high-speed signals; design techniques for signal integrity; the transmission-line concept; methods for temporal analysis and techniques for frequency domain analysis for connectics.

Surveys the electrical and layout perspectives of System-in-Package, the system integration technology that has emerged as a required technology to reduce the system board space and height in addition to the overall time-to-market and design cost of consumer electronics products such as those of cell phones, audio/video players and digital cameras.

This proceedings book presents selected papers from the 4th Conference on Signal and Information Processing, Networking and Computers (ICSINC) held in Qingdao, China on May 23–25, 2018. It focuses on the current research in a wide range of areas related to information theory, communication systems, computer science, signal processing, aerospace technologies, and other related technologies. With contributions from experts from both academia and industry, it is a valuable resource anyone interested in this field.

"The increasing demand for high-speed transport of data has revitalized optical communications, leading to extensive work on high-speed device and circuit design. This book deals with the design of high-speed integrated circuits for optical communicationtransceivers.Building upon a detailed understanding of optical devices, the book describes the analysis and design of critical building blocks, such as transimpedance and limiting amplifiers, laser drivers, phase-locked loops, oscillators, clock and datarecovery circuits, and multiplexers.This second edition of this best selling textbook has been updated to provide information on the latest developments in the field"--

Modeling and Design of Electromagnetic Compatibility for High-Speed Printed Circuit Boards and Packaging presents the electromagnetic modelling and design of three major electromagnetic compatibility (EMC) issues related to the high-speed printed circuit board (PCB) and electronic packages: signal integrity (SI), power integrity (PI),

and electromagnetic interference (EMI). The emphasis is put on two essential passive components of PCBs and packages: the power distribution network and the signal distribution network. This book includes two parts. Part one talks about the field-circuit hybrid methods used for the EMC modeling, including the modal method, the integral equation method, the cylindrical wave expansion method and the de-embedding method. Part two illustrates EMC design methods and explores the applications of novel metamaterials and two-dimensional materials on traditional EMC problems. This book is designed to enhance worthwhile electromagnetic theory and mathematical methods for practical engineers and to train students with advanced EMC applications.
This leading-edge circuit design resource offers the knowledge needed to quickly pinpoint transmission problems that can compromise circuit design. Discusses both design and debug issues at gigabit per second data rates.
Designing a complex ASIC/SoC is similar to learning a new language to start with and ultimately creating a masterpiece using experience, imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction. Some of it will come from experience, and some will come with concerted effort. Graduating from college and entering into the world of digital system design becomes an overwhelming task, as not all the information is readily available. In this book, we

have made an effort to explain the concepts in a simple way with real-world examples in Verilog. The book is intended for digital and system design engineers with emphasis on design and system architecture. The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11 through 20, focusing on the system aspects of chip design. This book can be used by students taking digital design and chip design courses in college and availing it as a guide in their professional careers. Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable design (parameterized design, functions, and generate structure). Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining larger building blocks such as LFSR, scrambler/descramblers, error detection and correction, parity, CRC, Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques. Chapter 7 and 8 bring in advanced concepts in chip design and architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and implementation. Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, portioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM.

It also covers good design practices, things to avoid and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols. Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA controller design that explains the scatter-gather DMA concept. Chapter12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging. Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation). Chapter 17 talks about Power Management protocols such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and lane reversal. Chapter 19 and 20 are devoted to serial bus protocols (PCI Express, Serial ATA, USB, Thunderbolt, and Ethernet) and their operation.

This second edition of An Engineer's Guide to Automated Testing of High-Speed Interfaces provides updates to reflect current state-of-the-art high-speed digital testing with automated test equipment technology (ATE). Featuring clear examples, this one-stop reference covers all critical aspects of automated testing, including an introduction to high-speed digital basics, a discussion of industry standards, ATE and bench instrumentation for digital applications, and test and measurement techniques for characterization and production environment. Engineers learn how to apply automated test equipment for testing high-speed digital I/O interfaces and gain a better understanding of PCI-Express 4, 100Gb Ethernet, and MIPI while exploring the correlation between phase noise and jitter. This updated resource provides expanded material on 28/32 Gbps NRZ testing and wireless testing that are becoming increasingly more pertinent for future applications. This book explores the current trend of merging high-speed digital testing within the fields of photonic and wireless testing. New System-Level Techniques for Optimizing Signal/Power Integrity in High-Speed Interfaces--from Pioneering Innovators at Rambus, Stanford, Berkeley, and MIT As data communication rates accelerate well into the multi-gigahertz range, ensuring signal integrity both on- and off-chip has become crucial. Signal integrity can no longer be addressed solely through improvements in package or board-level design: Diverse engineering teams must work together closely from the earliest design stages to identify the best system-level solutions. In High-Speed Signaling, several of the field’s most

respected practitioners and researchers introduce cutting-edge modeling, simulation, and optimization techniques for meeting this challenge. Edited by pioneering experts Drs. Dan Oh and Chuck Yuan, these contributors explain why noise and jitter are no longer separable, demonstrate how to model their increasingly complex interactions, and thoroughly introduce a new simulation methodology for predicting link-level performance with unprecedented accuracy. The authors address signal integrity from architecture through high-volume production, thoroughly discussing design, implementation, and verification. Coverage includes New advances in passive-channel modeling, power-supply noise and jitter modeling, and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high-volume manufacturing Practical, stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on-chip measurement techniques for in-situ link performance testing Trends and future directions in signal integrity engineering High-Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high-tech companies and universities: approaches that have never before been presented with this much practical detail. It will be invaluable to everyone concerned with signal integrity, including signal and power integrity engineers, high-speed I/O circuit designers, and

system-level board design engineers.

The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect each bit of the datapath from one chip to the next chip. Once upon a time this was an acceptable approach. However, one aspect (and perhaps the only aspect) of chip design which has not changed during the career of the authors is Moore's Law, which has dictated substantial increases in the number of circuits that can be manufactured on a chip. The pin densities of chip packaging technologies have not increased at the same pace as has silicon density, and this has led to a prevalence of High Speed Serdes (HSS) devices as an inherent part of almost any chip design. HSS devices are the dominant form of input/output for many (if not most) high-integration chips, moving serial data between chips at speeds up to 10 Gbps and beyond. Chip designers with a background in digital logic design tend to view HSS devices as simply complex digital input/output cells. This view ignores the complexity associated with serially moving billions of bits of data per second. At these data rates, the assumptions associated with digital signals break down and analog factors demand consideration. The chip designer who oversimplifies the problem does so at his or her own peril.

"This book covers a great variety of topics such as materials, environment, electronics, and computing, offering a vital source of information detailing the latest architectures, frameworks, methodologies, and research on energy-aware systems and networking for sustainable initiatives"--

This book describes recent research on terahertz CMOS design for high-speed wireless communication. The topics covered include fundamental technologies for terahertz CMOS

design, amplifier design, physical design approaches, transceiver design, and future prospects.
State-of-the-art JNB and SI Problem-Solving: Theory, Analysis, Methods, and Applications
Jitter, noise, and bit error (JNB) and signal integrity (SI) have become today‘s greatest challenges in high-speed digital design. Now, there’s a comprehensive and up-to-date guide to overcoming these challenges, direct from Dr. Mike Peng Li, cochair of the PCI Express jitter standard committee. One of the field’s most respected experts, Li has brought together the latest theory, analysis, methods, and practical applications, demonstrating how to solve difficult JNB and SI problems in both link components and complete systems. Li introduces the fundamental terminology, definitions, and concepts associated with JNB and SI, as well as their sources and root causes. He guides readers from basic math, statistics, circuit and system models all the way through final applications. Emphasizing clock and serial data communications applications, he covers JNB and SI simulation, modeling, diagnostics, debugging, compliance testing, and much more.
Analog Circuit Design contains the contribution of 18 tutorials of the 17th workshop on Advances in Analog Circuit Design. Each part discusses a specific to-date topic on new and valuable design ideas in the area of analog circuit design. Each part is presented by six experts in that field and state of the art information is shared and overviewed. This book is number 17 in this successful series of Analog Circuit Design.
High-Speed Signal Propagation: Advanced Black Magic brings together state-of-the-art techniques for building digital devices that can transmit faster and farther than ever before. Dr. Howard Johnson presents brand-new examples and design guidance, and a complete, unified theory of signal propagation for all metallic media. Coverage includes: understanding signal

impairments; managing speed/distance tradeoffs; differential signaling; inter-cabinet connections; clock distribution; simulation, and much more.

Presenting the cutting-edge results of new device developments and circuit implementations, High-Speed Devices and Circuits with THz Applications covers the recent advancements of nano devices for terahertz (THz) applications and the latest high-speed data rate connectivity technologies from system design to integrated circuit (IC) design, providing relevant standard activities and technical specifications. Featuring the contributions of leading experts from industry and academia, this pivotal work: Discusses THz sensing and imaging devices based on nano devices and materials Describes silicon on insulator (SOI) multigate nanowire field-effect transistors (FETs) Explains the theory underpinning nanoscale nanowire metal-oxide-semiconductor field-effect transistors (MOSFETs), simulation methods, and their results Explores the physics of the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT), as well as commercially available SiGe HBT devices and their applications Details aspects of THz IC design using standard silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices, including experimental setups for measurements, detection methods, and more An essential text for the future of high-frequency engineering, High-Speed Devices and Circuits with THz Applications offers valuable insight into emerging technologies and product possibilities that are attractive in terms of mass production and compatibility with current manufacturing facilities.

The Analog to Digital Converters represent one half of the link between the world we live in - analog - and the digital world of computers, which can handle the computations required in digital signal processing. These devices are mathematically very complex due to their

nonlinear behavior and thus fairly difficult to analyze without the use of simulation tools. High Speed A/D Converters: Understanding Data Converters Through SPICE presents the subject from the practising engineer's point of view rather than from the academic's point of view. A practical approach is emphasized. High Speed A/D Converters: Understanding Data Converters Through SPICE is intended as a learning tool by providing building blocks that can be stacked on top of each other to build higher order systems. The book provides a guide to understanding the various topologies used in A/D converters by suggesting simple methods for the blocks used in an A/D converter. The converters discussed throughout the book constitute a class of devices called undersampled or Nyquist converters. The tools used in deriving the results presented are: TopSpice® by Penzar - a mixed mode SPICE simulator - version 5.90. The files included in Appendix A were written for this tool. However, most circuit files need only minor adjustments to be used on other SPICE simulators such as PSpice, Hspice, IS_Spice and Micro-Cap IV; Mathcad 2000 - Professional by Mathsoft. This tool is very useful in performing FFT analysis as well as drawing some of the graphs. Again, the mathcad files are included to help the user analyze the data. High Speed A/D Converters: Understanding Data Converters Through SPICE not only supplies the models for the A/D converters for SPICE program but also describes the physical reasons for the converter's performance.

This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test, VDAT 2017, held in Roorkee, India, in June/July 2017. The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions. The papers were organized in topical sections named: digital design; analog/mixed signal; VLSI testing; devices and technology; VLSI architectures; emerging

technologies and memory; system design; low power design and test; RF circuits; architecture and CAD; and design verification.

The superabundance of data that is created by today's businesses is making storage a strategic investment priority for companies of all sizes. As storage takes precedence, the following major initiatives emerge: Flatten and converge your network: IBM® takes an open, standards-based approach to implement the latest advances in the flat, converged data center network designs of today. IBM Storage solutions enable clients to deploy a high-speed, low-latency Unified Fabric Architecture. Optimize and automate virtualization: Advanced virtualization awareness reduces the cost and complexity of deploying physical and virtual data center infrastructure. Simplify management: IBM data center networks are easy to deploy, maintain, scale, and virtualize, delivering the foundation of consolidated operations for dynamic infrastructure management. Storage is no longer an afterthought. Too much is at stake. Companies are searching for more ways to efficiently manage expanding volumes of data, and to make that data accessible throughout the enterprise. This demand is propelling the move of storage into the network. Also, the increasing complexity of managing large numbers of storage devices and vast amounts of data is driving greater business value into software and services. With current estimates of the amount of data to be managed and made available increasing at 60% each year, this outlook is where a storage area network (SAN) enters the arena. SANs are the leading storage infrastructure for the global economy of today. SANs offer simplified storage management, scalability, flexibility, and availability; and improved data access, movement, and backup. Welcome to the cognitive era. The smarter data center with the improved economics of IT can be achieved by connecting servers and storage with a high-

speed and intelligent network fabric. A smarter data center that hosts IBM Storage solutions can provide an environment that is smarter, faster, greener, open, and easy to manage. This IBM® Redbooks® publication provides an introduction to SAN and Ethernet networking, and how these networks help to achieve a smarter data center. This book is intended for people who are not very familiar with IT, or who are just starting out in the IT world.

Learn how automotive Ethernet is revolutionizing in-car networking from the experts at the core of its development. Providing an in-depth account of automotive Ethernet, from its background and development, to its future prospects, this book is ideal for industry professionals and academics alike.

Field Programmable Gate Arrays (FPGAs) are currently recognized as the most suitable platform for the implementation of complex digital systems targeting an increasing number of industrial electronics applications. They cover a huge variety of application areas, such as: aerospace, food industry, art, industrial automation, automotive, biomedicine, process control, military, logistics, power electronics, chemistry, sensor networks, robotics, ultrasound, security, and artificial vision. This book first presents the basic architectures of the devices to familiarize the reader with the fundamentals of FPGAs before identifying and discussing new resources that extend the ability of the devices to solve problems in new application domains. Design methodologies are discussed and application examples are included for some of these domains, e.g., mechatronics, robotics, and power systems.

Synthesising fifteen years of research, this authoritative text provides a comprehensive treatment of two major technologies for wireless chip and module interface design, covering technology fundamentals, design considerations and tradeoffs, practical implementation

considerations, and discussion of practical applications in neural network, reconfigurable processors, and stacked SRAM. It explains the design principles and applications of two near-field wireless interface technologies for 2.5-3D IC and module integration respectively, and describes system-level performance benefits, making this an essential resource for researchers, professional engineers and graduate students performing research in next-generation wireless chip and module interface design.