Embedded Computing A Vliw Approach To Architecture Compilers And Tools 1st Edition By Fisher Joseph A Faraboschi Paolo Young Cliff 2004 Hardcover

Embedded Computing for High Performance: Design Exploration and Customization Using High-level Compilation and Synthesis Tools provides a set of real-life example implementations that migrate traditional desktop systems to embedded systems. Working with popular hardware, including Xilinx and ARM, the book offers a comprehensive description of techniques for mapping computations expressed in programming languages such as C or MATLAB to high-performance embedded architectures consisting of multiple CPUs, GPUs, and reconfigurable hardware (FPGAs). The authors demonstrate a domain-specific language (LARA) that facilitates retargeting to multiple computing systems using the same source code. In this way, users can decouple original application code from transformed code and enhance productivity and program portability. After reading this book, engineers will understand the processes, methodologies, and best practices needed for the development of applications for high-performance embedded computing systems. Focuses on maximizing performance while managing energy consumption in embedded systems Explains how to retarget code for heterogeneous systems with GPUs and FPGAs Demonstrates a domain-specific language that facilitates migrating and retargeting existing applications to modern systems Includes downloadable slides, tools, and tutorials

This book is a summary of more than a decade of research in the area of backend optimization. It contains the latest fundamental research results in this field. While existing books are often more oriented toward Masters students, this book is aimed more towards professors and researchers as it contains more advanced subjects. It is unique in the sense that it contains information that has not previously been covered by other books in the field, with chapters on phase ordering in optimizing compilation; register saturation in instruction level parallelism; code size reduction for software pipelining; memory hierarchy effects and instruction level parallelism. Other chapters provide the latest research results in well-known topics such as register need, and software pipelining and periodic register allocation.

Here is an extremely useful book that provides insight into a number of different flavors of processor architectures and their design, software tool generation, implementation, and verification. After a brief introduction to processor architectures and how processor designers have sometimes failed to deliver what was expected, the authors introduce a generic flow for embedded on-chip processor design and start to explore the vast design space of on-chip processing. The authors cover a number of different types of processor core.

COMPUTER ORGANIZATION AND ARCHITECTURE: THEMES AND VARIATIONS stresses the structure of the complete system (CPU, memory, buses and peripherals) and reinforces that core content with an emphasis on divergent examples. This approach to computer architecture is an effective arrangement that provides sufficient detail at the logic and organizational levels appropriate for EE/ECE departments as well as for Computer Science readers. The text goes well beyond the minimal curriculum coverage and introduces topics that are important to anyone involved with computer architecture in a way that is both thought provoking and interesting to all. Important Notice: Media content referenced within the product description or the product text may not be available in the ebook version.

Computing Handbook, Third Edition: Computer Science and Software Engineering mirrors the modern taxonomy of computer science and software engineering as described by the Association for Computing Machinery (ACM) and the IEEE Computer Society (IEEE-CS). Written by established leading experts and influential young researchers, the first volume of this popular handbook examines the elements involved in designing and implementing software, new areas in which computers are being used, and ways to solve computing problems. The book also explores our current understanding of software engineering and its effect on the practice of software development and the education of software professionals. Like the second volume, this first volume describes what occurs in research laboratories, educational institutions, and public and private organizations to advance the effective development and use of computers and computing in today’s world. Research-level survey articles provide deep insights into the computing discipline, enabling readers to understand the principles and practices that drive computing education, research, and development in the twenty-first century.

This book contains extended and revised versions of the best papers presented at the 21st IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2013, held in Istanbul, Turkey, in October 2013. The 11 papers included in the book were carefully reviewed and selected from the 48 full papers presented at the conference. An extended version of a previously unpublished high-quality paper from VLSI-SoC 2012 is also included. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.

This two-volume-set constitutes the refereed proceedings of the 6th International Conference on Future Information Technology, FutureTech 2011, held in Crete, Greece, in June 2011. The 123 revised full papers presented in both volumes were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on future information technology, IT service and cloud computing; social computing, network, and services; forensics for future generation communication environments; intelligent transportation systems and applications; multimedia and semantic technologies; information science and technology.

This book presents a novel approach for Architecture Description Language (ADL)-based instruction-set description that enables the automatic retargeting of the complete software toolkit from a single ADL processor model.

Embedded ComputingA VLIW Approach to Architecture, Compilers and ToolsElsevier

The LNCS series reports state-of-the-art results in computer science research, development, and education, at a high level and in both printed and electronic form. Enjoying tight cooperation with the R&D community, with numerous individuals, as well as with prestigious organizations and societies, LNCS has grown into the most comprehensive computer science research forum available. The scope of LNCS, including its subseries LNAI and LNBI, spans the whole range of computer science and information technology including interdisciplinary topics in a variety of application fields. In parallel to the printed book, each new volume is published electronically in LNCS Online.

It gives me immense pleasure to introduce this timely handbook to the research/- velopment communities in the ?eld of

signal processing systems (SPS). This is the ?rst of its kind and represents state-of-the-arts coverage of research in this ?eld. The driving force behind information technologies (IT) hinges critically upon the major advances in both component integration and system integration. The major breakthrough for the former is undoubtedly the invention of IC in the 50's by Jack S. Kilby, the Nobel Prize Laureate in Physics 2000. In an integrated circuit, all components were made of the same semiconductor material. Beginning with the pocket calculator in 1964, there have been many increasingly complex applications followed. In fact, processing gates and memory storage on a chip have since then grown at an exponential rate, following Moore's Law. (Moore himself admitted that Moore's Law had turned out to be more accurate, longer lasting and deeper in impact than he ever imagined.) With greater device integration, various signal processing systems have been realized for many killer IT applications. Further breakthroughs in computer sciences and Internet technologies have also catalyzed large-scale system integration. All these have led to today's IT revolution which has profound impacts on our lifestyle and overall prospect of humanity. (It is hard to imagine life today without mobiles or Internets!) The success of SPS requires a well-concerted integrated approach from mul- ple disciplines, such as device, design, and application.

Containing over 300 entries in an A-Z format, the Encyclopedia of Parallel Computing provides easy, intuitive access to relevant information for professionals and researchers seeking access to any aspect within the broad field of parallel computing. Topics for this comprehensive reference were selected, written, and peer-reviewed by an international pool of distinguished researchers in the field. The Encyclopedia is broad in scope, covering machine organization, programming languages, algorithms, and applications. Within each area, concepts, designs, and specific implementations are presented. The highly-structured essays in this work comprise synonyms, a definition and discussion of the topic, bibliographies, and links to related literature. Extensive cross-references to other entries within the Encyclopedia support efficient, user-friendly searchers for immediate access to useful information. Key concepts presented in the Encyclopedia of Parallel Computing include; laws and metrics; specific numerical and non-numerical algorithms; asynchronous algorithms; libraries of subroutines; benchmark suites; applications; sequential consistency and cache coherency; machine classes such as clusters, shared-memory multiprocessors, special-purpose machines and dataflow machines; specific machines such as Cray supercomputers, IBM's cell processor and Intel's multicore machines; race detection and auto parallelization; parallel programming languages, synchronization primitives, collective operations, message passing libraries, checkpointing, and operating systems. Topics covered: Speedup, Efficiency, Isoefficiency, Redundancy, Amdahls law, Computer Architecture Concepts, Parallel Machine Designs, Benmarks, Parallel Programming concepts & design, Algorithms, Parallel applications. This authoritative reference will be published in two formats: print and online. The online edition features hyperlinks to cross-references and to additional significant research. Related Subjects: supercomputing, high-performance computing, distributed computing

This book introduces a novel design methodology which can significantly reduce the ASIP development effort through high degrees of design automation. The key elements of this new design methodology are a powerful application profiler and an automated instruction-set customization tool which considerably lighten the burden of mapping a target application to an ASIP architecture in the initial design stages. The book includes several design case studies with real life embedded applications to demonstrate how the methodology and the tools can be used in practice for accelerating the overall ASIP design process.

A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 1 covers the key components of MPSoC: processors, memory, interconnect and interfaces. It describes advance features of these components and technologies to build efficient MPSoC architectures. All the main components are detailed: use of memory and their technology, communication support and consistency, and specific processor architectures for general purposes or for dedicated applications.

The fact that there are more embedded computers than general-purpose computers and that we are impacted by hundreds of them every day is no longer news. What is news is that their increasing performance requirements, complexity and capabilities demand a new approach to their design. Fisher, Faraboschi, and Young describe a new age of embedded computing design, in which the processor is central, making the approach radically distinct from contemporary practices of embedded systems design. They demonstrate why it is essential to take a computing-centric and system-design approach to the traditional elements of nonprogrammable components, peripherals, interconnects and buses. These elements must be unified in a system design with high-performance processor architectures, microarchitectures and compilers, and with the compilation tools, debuggers and simulators needed for application development. In this landmark text, the authors apply their expertise in highly interdisciplinary hardware/software development and VLIW processors to illustrate this change in embedded computing. VLIW architectures have long been a popular choice in embedded systems design, and while VLIW is a running theme throughout the book, embedded computing is the core topic. Embedded Computing examines both in a book filled with fact and opinion based on the authors many years of R&D experience. · Complemented by a unique, professional-quality embedded tool-chain on the authors' website, http://www.vliw.org/book · Combines technical depth with real-world experience · Comprehensively explains the differences between general purpose computing systems and embedded systems at the hardware, software, tools and operating system levels. · Uses concrete examples to explain and motivate the trade-offs.

This book constitutes the refereed proceedings of the Second International Conference on Computability in Europe, CiE

2006, held in Swansea, UK, June/July 2006. The book presents 31 revised full papers together with 30 invited papers, including papers corresponding to 8 plenary talks and 6 special sessions on proofs and computation, computable analysis, challenges in complexity, foundations of programming, mathematical models of computers and hypercomputers, and Gödel centenary: Gödel's legacy for computability.

Nowadays, embedded systems - the computer systems that are embedded in various kinds of devices and play an important role of specific control functions, have permitted various aspects of industry. Therefore, we can hardly discuss our life and society from now onwards without referring to embedded systems. For wide-ranging embedded systems to continue their growth, a number of high-quality fundamental and applied researches are indispensable. This book contains 19 excellent chapters and addresses a wide spectrum of research topics on embedded systems, including basic researches, theoretical studies, and practical work. Embedded systems can be made only after fusing miscellaneous technologies together. Various technologies condensed in this book will be helpful to researchers and engineers around the world.

This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2012, held in Santa Cruz, CA, USA, in October 2012. The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.

This volume constitutes the refereed proceedings of the 7th International Conference on Modelling and Development of Intelligent Systems, MDIS 2020, held in Sibiu, Romania, in October 2020. Due to the COVID-19 pandemic the conference was held online. The 25 revised full papers presented in the volume were carefully reviewed and selected from 57 submissions. The papers are organized in topical sections on evolutionary computing; intelligent systems for decision support; machine learning; mathematical models for development of intelligent systems; modelling and optimization of dynamic systems; ontology engineering.

This book constitutes the thoroughly refereed conference proceedings of the 9th International Symposium on Reconfigurable Computing: Architectures, Tools and Applications, ARC 2013, held in Los Angeles, CA, USA, in March 2013. The 28 revised papers presented, consisting of 20 full papers and 11 poster papers were carefully selected from 41 submissions. The topics covered are applications, arithmetic, design optimization for FPGAs, architectures, place and routing.

Customizable processors have been described as the next natural step in the evolution of the microprocessor business: a step in the life of a new technology where top performance alone is no longer sufficient to guarantee market success. Other factors become fundamental, such as time to market, convenience, energy efficiency, and ease of customization. This book is the first to explore comprehensively one of the most fundamental trends which emerged in the last decade: to treat processors not as rigid, fixed entities, which designers include “as is in their products; but rather, to build sound methodologies to tailor-fit processors to the specific needs of such products. This book addresses the goal of maintaining a very large family of processors, with a wide range of features, at a cost comparable to that of maintaining a single processor. First book to present comprehensively the major ASIP design methodologies and tools without any particular bias Written by most of the pioneers and top international experts of this young domain Unique mix of management perspective, technical detail, research outlook, and practical implementation

It is our great pleasure to present the proceedings of the second Russia–Taiwan Symposium on Methods and Tools of Parallel Programming (MTPP 2010). MTPP is the main regular event of the Russia–Taiwan scientific forum that covers the many dimensions of methods and tools of parallel programming, algorithms and architectures, encompassing fundamental theoretical approaches, practical experimental projects, and commercial components and systems. As applications of computing systems have permeated every aspect of daily life, the power of computing systems has become increasingly critical. Therefore, MTPP is intended to play an important role allowing researchers to exchange information regarding advancements in the state of the art and practice of IT-driven services and applications, as well as to identify emerging research topics and define the future directions of parallel computing. We received a large number of high-quality submissions this year. In the first stage, all papers submitted were screened for their relevance and general submission requirements. These manuscripts then underwent a rigorous peer-review process with at least three reviewers per paper. At the end, 33 papers were accepted for presentation and included in the main proceedings. To encourage and promote the work presented at MTPP 2010, we are delighted to inform the authors that some of the papers will be accepted in special issues of the Journal of Supercomputing, which has played a prominent role in promoting the development and use of parallel and distributed processing.

Computers as Components, Second Edition, updates the first book to bring essential knowledge on embedded systems technology and techniques under a single cover. This edition has been updated to the state-of-the-art by reworking and expanding performance analysis with more examples and exercises, and coverage of electronic systems now focuses on the latest applications. It gives a more comprehensive view of multiprocessors including VLIW and superscalar architectures as well as more detail about power consumption. There is also more advanced treatment of all the components of the system as well as in-depth coverage of networks, reconfigurable systems, hardware-software co-design, security, and program analysis. It presents an updated discussion of current industry development software including Linux and Windows CE. The new edition's case studies cover SHARC DSP with the TI C5000 and C6000 series, and real-world applications such as DVD players and cell phones. Researchers, students, and savvy professionals schooled in hardware or software design, will value Wayne Wolf's integrated engineering design approach. * Uses real processors (ARM processor and TI C55x DSP) to demonstrate both technology and techniques...Shows readers how to apply principles to actual design practice. * Covers all necessary topics with emphasis on actual design practice...Realistic introduction to the state-of-the-art for both students and practitioners. * Stresses necessary fundamentals which can be applied to evolving technologies...helps readers gain facility to design large, complex embedded systems that actually work.

Intelligent readers who want to build their own embedded computer systems-- installed in everything from cell phones to cars to handheld organizers to refrigerators-- will find this book to be the most in-depth, practical, and up-to-date guide on the market. Designing Embedded Hardware carefully steers between the practical and philosophical aspects, so developers can both create

their own devices and gadgets and customize and extend off-the-shelf systems. There are hundreds of books to choose from if you need to learn programming, but only a few are available if you want to learn to create hardware. Designing Embedded Hardware provides software and hardware engineers with no prior experience in embedded systems with the necessary conceptual and design building blocks to understand the architectures of embedded systems. Written to provide the depth of coverage and real-world examples developers need, Designing Embedded Hardware also provides a road-map to the pitfalls and traps to avoid in designing embedded systems. Designing Embedded Hardware covers such essential topics as: The principles of developing computer hardware Core hardware designs Assembly language concepts Parallel I/O Analog-digital conversion Timers (internal and external) UART Serial Peripheral Interface Inter-Integrated Circuit Bus Controller Area Network (CAN) Data Converter Interface (DCI) Low-power operation This invaluable and eminently useful book gives you the practical tools and skills to develop, build, and program your own application-specific computers.

This book precisely formulates and simplifies the presentation of Instruction Level Parallelism (ILP) compilation techniques. It uniquely offers consistent and uniform descriptions of the code transformations involved. Due to the ubiquitous nature of ILP in virtually every processor built today, from general purpose CPUs to application-specific and embedded processors, this book is useful to the student, the practitioner and also the researcher of advanced compilation techniques. With an emphasis on fine-grain instruction level parallelism, this book will also prove interesting to researchers and students of parallelism at large, in as much as the techniques described yield insights that go beyond superscalar and VLIW (Very Long Instruction Word) machines compilation and are more widely applicable to optimizing compilers in general. ILP techniques have found wide and crucial application in Design Automation, where they have been used extensively in the optimization of performance as well as area and power minimization of computer designs.

This book constitutes the second part of the refereed proceedings of the Third International Conference, IC3 2010, held in Noida, India, in August 2010. The 23 revised full papers presented were carefully reviewed and selected from numerous submissions.

This book explores break-through approaches to tackling and mitigating the well-known problems of compiler optimization using design space exploration and machine learning techniques. It demonstrates that not all the optimization passes are suitable for use within an optimization sequence and that, in fact, many of the available passes tend to counteract one another. After providing a comprehensive survey of currently available methodologies, including many experimental comparisons with state-of-the-art compiler frameworks, the book describes new approaches to solving the problem of selecting the best compiler optimizations and the phase-ordering problem, allowing readers to overcome the enormous complexity of choosing the right order of optimizations for each code segment in an application. As such, the book offers a valuable resource for a broad readership, including researchers interested in Computer Architecture, Electronic Design Automation and Machine Learning, as well as computer architects and compiler developers.

Here is a laboratory workbook filled with interesting and challenging projects for digital logic design and embedded systems classes. The workbook introduces you to fully integrated modern CAD tools, logic simulation, logic synthesis using hardware description languages, design hierarchy, current generation field programmable gate array technology, and SoPC design. Projects cover such areas as serial communications, state machines with video output, video games and graphics, robotics, pipelined RISC processor cores, and designing computer systems using a commercial processor core.

The present book includes extended and revised versions of papers presented during the 2018 International Computer Symposium (ICS 2018), held in Yunlin, Republic of China (Taiwan), on December 20-22, 2018. The 86 papers presented were carefully reviewed and selected from 263 submissions from 11 countries. The variety of the topics include machine learning, sensor devices and platforms, sensor networks, robotics, embedded systems, networks, operating systems, software system structures, database design and models, multimedia and multimodal retrieval, object detection, image processing, image compression, mobile and wireless security.

Modern consumers carry many electronic devices, like a mobile phone, digital camera, GPS, PDA and an MP3 player. The functionality of each of these devices has gone through an important evolution over recent years, with a steep increase in both the number of features as in the quality of the services that they provide. However, providing the required compute power to support (an uncompromised combination of) all this functionality is highly non-trivial. Designing processors that meet the demanding requirements of future mobile devices requires the optimization of the embedded system in general and of the embedded processors in particular, as they should strike the correct balance between flexibility, energy efficiency and performance. In general, a designer will try to minimize the energy consumption (as far as needed) for a given performance, with a sufficient flexibility. However, achieving this goal is already complex when looking at the processor in isolation, but, in reality, the processor is a single component in a more complex system. In order to design such complex system successfully, critical decisions during the design of each individual component should take into account effect on the other parts, with a clear goal to move to a global Pareto optimum in the complete multi-dimensional exploration space. In the complex, global design of battery-operated embedded systems, the focus of Ultra-Low Energy Domain-Specific Instruction-Set Processors is on the energy-aware architecture exploration of domain-specific instruction-set processors and the co-optimization of the datapath architecture, foreground memory, and instruction memory organisation with a link to the required mapping techniques or compiler steps at the early stages of the design. By performing an extensive energy breakdown experiment for a complete embedded platform, both energy and performance bottlenecks have been identified, together with the important relations between the different components. Based on this knowledge, architecture extensions are proposed for all the bottlenecks.

This book constitutes the refereed proceedings of the 8th International Symposium on Reconfigurable Computing: Architectures, Tools and Applications, ARC 2012, held in Hongkong, China, in March 2012. The 35 revised papers presented, consisting of 25 full papers and 10 poster papers were carefully reviewed and selected from 44 submissions. The topics covered are applied RC design methods and tools, applied RC architectures, applied RC applications and critical issues in applied RC.

Nowadays, the prevalence of computing systems in our lives is so ubiquitous that we live in a cyber-physical world dominated by computer systems, from pacemakers to cars and airplanes. These systems demand for more computational performance to process large amounts of data from multiple data sources with guaranteed processing times. Actuating outside of the required timing bounds may cause the failure of the system, being vital for systems like planes, cars, business monitoring, e-trading, etc. High-Performance and Time-Predictable Embedded Computing presents recent advances in software architecture and tools to support such complex systems, enabling the design of embedded computing devices which are able to deliver high-performance

whilst guaranteeing the application required timing bounds. Technical topics discussed in the book include: Parallel embedded platformsProgramming modelsMapping and scheduling of parallel computationsTiming and schedulability analysisRuntimes and operating systems The work reflected in this book was done in the scope of the European project P?SOCRATES, funded under the FP7 framework program of the European Commission. High-performance and time-predictable embedded computing is ideal for personnel in computer/communication/embedded industries as well as academic staff and master/research students in computer science, embedded systems, cyber-physical systems and internet-of-things.

Until the late 1980s, information processing was associated with large mainframe computers and huge tape drives. During the 1990s, this trend shifted toward information processing with personal computers, or PCs. The trend toward miniaturization continues and in the future the majority of information processing systems will be small mobile computers, many of which will be embedded into larger products and interfaced to the physical environment. Hence, these kinds of systems are called embedded systems. Embedded systems together with their physical environment are called cyber-physical systems. Examples include systems such as transportation and fabrication equipment. It is expected that the total market volume of embedded systems will be significantly larger than that of traditional information processing systems such as PCs and mainframes. Embedded systems share a number of common characteristics. For example, they must be dependable, efficient, meet real-time constraints and require customized user interfaces (instead of generic keyboard and mouse interfaces). Therefore, it makes sense to consider common principles of embedded system design. Embedded System Design starts with an introduction into the area and a survey of specification models and languages for embedded and cyber-physical systems. It provides a brief overview of hardware devices used for such systems and presents the essentials of system software for embedded systems, like real-time operating systems. The book also discusses evaluation and validation techniques for embedded systems. Furthermore, the book presents an overview of techniques for mapping applications to execution platforms. Due to the importance of resource efficiency, the book also contains a selected set of optimization techniques for embedded systems, including special compilation techniques. The book closes with a brief survey on testing. Embedded System Design can be used as a text book for courses on embedded systems and as a source which provides pointers to relevant material in the area for PhD students and teachers. It assumes a basic knowledge of information processing hardware and software. Courseware related to this book is available at http://ls12-www.cs.tu-dortmund.de/~marwedel.

An introduction to the engineering principles of embedded systems, with a focus on modeling, design, and analysis of cyber-physical systems. The most visible use of computers and software is processing information for human consumption. The vast majority of computers in use, however, are much less visible. They run the engine, brakes, seatbelts, airbag, and audio system in your car. They digitally encode your voice and construct a radio signal to send it from your cell phone to a base station. They command robots on a factory floor, power generation in a power plant, processes in a chemical plant, and traffic lights in a city. These less visible computers are called embedded systems, and the software they run is called embedded software. The principal challenges in designing and analyzing embedded systems stem from their interaction with physical processes. This book takes a cyber-physical approach to embedded systems, introducing the engineering concepts underlying embedded systems as a technology and as a subject of study. The focus is on modeling, design, and analysis of cyber-physical systems, which integrate computation, networking, and physical processes. The second edition offers two new chapters, several new exercises, and other improvements. The book can be used as a textbook at the advanced undergraduate or introductory graduate level and as a professional reference for practicing engineers and computer scientists. Readers should have some familiarity with machine structures, computer programming, basic discrete mathematics and algorithms, and signals and systems.

Although multicore is now a mainstream architecture, there are few textbooks that cover parallel multicore architectures. Filling this gap, Fundamentals of Parallel Multicore Architecture provides all the material for a graduate or senior undergraduate course that focuses on the architecture of multicore processors. The book is also useful as a ref

This book constitutes the refereed proceedings of the 13th International Symposium on Applied Reconfigurable Computing, ARC 2017, held in Delft, The Netherlands, in April 2017. The 17 full papers and 11 short papers presented in this volume were carefully reviewed and selected from 49 submissions. They are organized in topical sections on adaptive architectures, embedded computing and security, simulation and synthesis, design space exploration, fault tolerance, FGPA-based designs, neural neworks, and languages and estimation techniques.

This book originated from a workshop held at the DATE 2005 conference, namely Designing Complex SOCs. State-of-the-art in issues related to System-on-Chip (SoC) design by leading experts in the fields, it covers IP development, verification, integration, chip implementation, testing and software. It contains valuable academic and industrial examples for those involved with the design of complex SOCs.

This book provides design methods for Digital Signal Processors and Application Specific Instruction set Processors, based on the author's extensive, industrial design experience. Top-down and bottom-up design methodologies are presented, providing valuable guidance for both students and practicing design engineers. Coverage includes design of internal-external data types, application specific instruction sets, micro architectures, including designs for datapath and control path, as well as memory sub systems. Integration and verification of a DSP-ASIP processor are discussed and reinforced with extensive examples. FOR INSTRUCTORS: To obtain access to the solutions manual for this title simply register on our textbook website (textbooks.elsevier.com)and request access to the Computer Science or Electronics and Electrical Engineering subject area. Once approved (usually within one business day) you will be able to access all of the instructor-only materials through the ";Instructor Manual"; link on this book's full web page. * Instruction set design for application specific processors based on fast application profiling * Micro architecture design methodology * Micro architecture design details based on real examples * Extendable architecture design protocols * Design for efficient memory sub systems (minimizing on chip memory and cost) * Real example designs based on extensive, industrial experiences.

High-Performance Embedded Computing, Second Edition, combines leading-edge research with practical guidance in a variety of embedded computing topics, including real-time systems, computer architecture, and low-power design. Author Marilyn Wolf presents a comprehensive survey of the state of the art, and guides you to achieve high levels of

performance from the embedded systems that bring these technologies together. The book covers CPU design, operating systems, multiprocessor programs and architectures, and much more. Embedded computing is a key component of cyber-physical systems, which combine physical devices with computational resources for control and communication. This revised edition adds new content and examples of cyber-physical systems throughout the book, including design methodologies, scheduling, and wide-area CPS to illustrate the possibilities of these new systems. Revised and updated with coverage of recently developed consumer electronics architectures and models of computing Includes new VLIW processors such as the TI Da Vinci, and CPU simulation Learn model-based verification and middleware for embedded systems Supplemental material includes lecture slides, labs, and additional resources

The extreme ?exibility of recon?gurable architectures and their performance pot- tial have made them a vehicle of choice in a wide range of computing domains, from rapid circuit prototyping to high-performance computing. The increasing availab- ity of transistors on a die has allowed the emergence of recon?gurable architectures with a large number of computing resources and interconnection topologies. To - ploit the potential of these recon?gurable architectures, programmers are forced to map their applications, typically written in high-level imperative programming l- guages, such as C or MATLAB, to hardware-oriented languages such as VHDL or Verilog. In this process, they must assume the role of hardware designers and software programmers and navigate a maze of program transformations, mapping, and synthesis steps to produce ef?cient recon?gurable computing implementations. The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process. It is thus widely believed that automatic compilation from high-level programming languages is the key to the success of recon?gurable computing. This book describes a wide range of code transformations and mapping te- niques for programs described in high-level programming languages, most - tably imperative languages, to recon?gurable architectures.

This book constitutes the refereed proceedings of the 6th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2006, held in Samos, Greece on July 2006. The 47 revised full papers presented together with 2 keynote talks were thoroughly reviewed and selected from 130 submissions. The papers are organized in topical sections on system design and modeling, wireless sensor networks, processor design, dependable computing, architectures and implementations, and embedded sensor systems.