

Digital Logic Design Question Bankslibforme

May 19, 2005 · hi guys, how to approach a logic design problem?? suppose I haf a IC which takes in 2 3-bit binary numbers, x_2, x_1, x_0 and y_2, y_1, y_0 .. determines whether they are equal and which 1 is larger there are 3 outputs defined as follows 1. $M=1$ only if 2 input numbers are equal 2. $N =1$ only if $x_2 x_1 x_0$

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Apr 12, 2016 · Question 10. Consider the following statements : (a) Boolean expressions and logic networks correspond to labelled acyclic digraphs. (b) Optimal boolean expressions may not correspond to simplest networks. (c) ...

Multiple choice Questions Digital Logic Design 1. How many bits must each word have in one-to-four line de-multiplexer to be implemented using ...

26. A multiplexer with 2^n data input lines requires ___ number of "control" or select lines to select the input line. Show Answer. 27. A 4: 1 Mux selects one of the input lines and connects it to the output line using 2 select lines. (State true or false) Show Answer. 28. Demultiplexer is ...

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Dec 16, 2013 · Hello, I'd appreciate your help with approaching this design question, faced in an interview: Plan a logical design which gets a single read/write bit every clock cycle, and a number. The design should store the histogram of the written input, and display it on a read command What is the

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Answer (1 of 13): There are no predefined Digital design interview questions as the person can ask anything starting from a simple concept to advance level and it also varies at different experience level. So it's better to get prepared all the concepts.However in ...

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This course covers the concepts of digital logic and switching networks. The course includes the fundamental concepts of boolean algebra and its application for circuit analysis, multilevel

gates networks, flip-flops, counters logic devices and synchronous and asynchronous sequential logic and digital integrated circuits.

Dec 31, 2018 · The digital logic design is a system in electrical and computer engineering that uses simple numerical values to produce input and output operations. As a digital design engineer, you may assist

Mealy FSM uses only input actions, i.e. output depends on input and state. The use of a Mealy FSM leads often to a reduction of the number of states. Moore FSM uses only entry actions, i.e. output depends only on the state. The advantage of the Moore model is ...

Digital Logic MCQ Question 17. Download Solution PDF. A 16-bit synchronous binary up-counter is clocked with a frequency f CLK. The two most significant bits are OR-ed together to form an output Y. Measurements show that Y is periodic, and the duration for which Y remains high in each period is 24 ms.

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Discuss ISRO CS 2013 Digital-Logic-Design Flip-flops Question 1 Explanation: Three stage counter with RS Flip Flop is 3 bit counter, so after every 8 clock pulse, it will return to initial state. and in the 9th pulse, the counter stage will exceed by 1

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