Design Constraints Sdc Now Xilinx Synthesis

The primary aim of this book is to introduce the concepts of FPGA timing based on Synopsys style timing analysis in a simplified yet concise way with emphasis on clear understanding of concepts and practical aspects away from syntax clutter or excessive sdc based examples.

Are you have a problem with Synopsys Design Constraints (SDC) or Altera Timing Analyzer? This book will have all the answers for you. It explains about each frequently-used SDC command, specify timing and other design constraints. With Altera time analyzer uses industrystandard constraint and analysis methodology to report on all data required times,data arrival times, and clock arrival times for all register-to-register.

Since register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

This book provides a single-source reference to the state-of-the-art in logic synthesis. Readers will benefit from the authors' expert perspectives on new technologies and logic synthesis, new data structures, big data and logic synthesis, and convergent logic synthesis. The authors describe techniques that will enable readers to take advantage of recent advances in big data techniques and frameworks in order to have better logic synthesis algorithms.

Synopsys Design ConstraintsSynopsys Design Constraints (SDC) Guide: Synopsys Design Constraints File Not Found

This book was written to arm engineers qualified and knowledgeable in the area of VLSI circuits with the essential knowledge they need to get into this exciting field and to help those already in it achieve a higher level of proficiency. Few people truly understand how a large chip is developed, but an understanding of the whole process is necessary to appreciate the importance of each part of it and to understand the process from concept to silicon. It will teach readers how to become better engineers through a practical approach of diagnosing and attacking real-world problems.

Verilog and its usage has come a long way since its original invention in the mid-80s by Phil Moorby. At the time the average design size was around ten thousand gates, and simulation to validate the design was its primary usage. But between then and now designs have increased dramatically in size, and automatic logic synthesis from RTL has become the standard design ?ow for most design. Indeed, the language has evolved and been re-standardized too.

Overtheyears,manybookshavebeenwrittenaboutVerilog.Myown,coauthored with Phil Moorby, had the goal of de?ning the language and its usage, providing - amples along the way. It has been updated with ?ve new editions as the language and its usage evolved. However this new book takes a very different and unique view; that of the designer. John Michael Williams has a long history of working and teaching in the ?eld of IC and ASIC design. He brings an indepth presentation of Verilog and how to use it with logic synthesis tools; no other Verilog book has dealt with this topic as deeply as he has. If you need to learn Verilog and get up to speed quickly to use it for synthesis, this book is for you. It is sectioned around a set of lessons including presentation and explanation of new concepts and approaches to design, along with lab sessions.

This book describes best practices for successful FPGA design. It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book's content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.

This book enables readers to achieve ultra-low energy digital system performance. The author's main focus is the energy consumption of microcontroller architectures in digital (sub)-systems. The book covers a broad range of topics extensively: from circuits through design strategy to system architectures. The result is a set of techniques and a context to realize minimum energy digital systems. Several prototype silicon implementations are discussed, which put the proposed techniques to the test. The achieved results demonstrate an extraordinary combination of variation-resilience, high speed performance and ultra-low energy.

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

This book includes the proceedings of the second International Conference on Advances in Computer Science and Engineering (CES 2012), which was held during January 13-14, 2012 in Sanya, China. The papers in these proceedings of CES 2012 focus on the researchers' advanced works in their fields of Computer Science and Engineering mainly organized in four topics, (1)

Software Engineering, (2) Intelligent Computing, (3) Computer Networks, and (4) Artificial Intelligence Software.
This book is designed both for FPGA users interested in developing new, specific components - generally for reducing execution times –and IP core designers interested in extending their catalog of specific components. The main focus is circuit synthesis and the discussion shows, for example, how a given algorithm executing some complex function can be translated to a synthesizable circuit description, as well as which are the best choices the designer can make to reduce the circuit cost, latency, or power consumption. This is not a book on algorithms. It is a book that shows how to translate efficiently an algorithm to a circuit, using techniques such as parallelism, pipeline, loop unrolling, and others. Numerous examples of FPGA implementation are described throughout this book and the circuits are modeled in VHDL. Complete and synthesizable source files are available for download.
Author Impact
This textbook for courses in Embedded Systems introduces students to necessary concepts, through a hands-on approach. It gives a great introduction to FPGA-based microprocessor system design using state-of-the-art boards, tools, and microprocessors from Altera/Intel® and Xilinx®. HDL-based designs (soft-core), parameterized cores (Nios II and MicroBlaze), and ARM Cortex-A9 design are discussed, compared and explored using many hand-on designs projects. Custom IP for HDMI coder, Floating-point operations, and FFT bit-swap are developed, implemented, tested and speed-up is measured. Downloadable files include all design examples such as basic processor synthesizable code for Xilinx and Altera tools for PicoBlaze, MicroBlaze, Nios II and ARMv7 architectures in VHDL and Verilog code, as well as the custom IP projects. Each Chapter has a substantial number of short quiz questions, exercises, and challenging projects. Explains soft, parameterized, and hard core systems design tradeoffs; Demonstrates design of popular KCPSM6 8 Bit microprocessor step-by-step; Discusses the 32 Bit ARM Cortex-A9 and a basic processor is synthesized; Covers design flows for both FPGA Market leaders Nios II Altera/Intel and MicroBlaze Xilinx system; Describes Compiler-Compiler Tool development; Includes a substantial number of Homework’s and FPGA exercises and design projects in each chapter.
Computer chip industry veteran Bartleson provides ideas for creating better standards, increasing respect for the standardization process, and ways for leveraging others' industry expertise to create more effective technical standards.
This book collects the best practices FPGA-based Prototyping of SoC and ASIC devices into one place for the first time, drawing upon not only the authors' own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future. The book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an FPGA-based prototyping project. We start by analyzing the challenges and benefits of FPGA-based Prototyping and how they compare to other prototyping methods. We present the current state of the available FPGA technology and tools and how to get started on a project. The FPMM also compares between home-made and outsourced FPGA platforms and how to analyze which will best meet the needs of a given project. The central chapters deal with implementing an SoC design in FPGA technology including clocking, conversion of memory, partitioning, multiplexing and handling IP amongst many other subjects. The important subject of bringing up the design on the FPGA boards is covered next, including the introduction of the real design into the board, running embedded software upon it in and debugging and iterating in a lab environment. Finally we explore how the FPGA-based Prototype can be linked into other verification methodologies, including RTL simulation and virtual models in SystemC. Along the way, the reader will discover that an adoption of FPGA-based Prototyping from the beginning of a project, and an approach we call Design-for-Prototyping, will greatly increase the success of the prototype and the whole SoC project, especially the embedded software portion. Design-for-Prototyping is introduced and explained and promoted as a manifesto for better SoC design. Readers can approach the subjects from a number of directions. Some will be experienced with many of the tasks involved in FPGA-based Prototyping but are looking for new insights and ideas; others will be relatively new to the subject but experienced in other verification methodologies; still others may be project leaders who need to understand if and how the benefits of FPGA-based prototyping apply to their next SoC project. We have tried to make each subject chapter relatively standalone, or where necessary, make numerous forward and backward references between subjects, and provide recaps of certain key subjects. We hope you like the book and we look forward to seeing you on the FPMM on-line community soon (go to www.synopsys.com/fpmm).
This book provides insight into the practical design of VLSI circuits. It is aimed at novice VLSI designers and other enthusiasts who would like to understand VLSI design flows. Coverage includes key concepts in CMOS digital design, design of DSP and communication blocks on FPGAs, ASIC front end and physical design, and analog and mixed signal design. The approach is designed to focus on practical implementation of key elements of the VLSI design process, in order to make the topic accessible to novices. The design concepts are demonstrated using software from Mathworks, Xilinx, Mentor Graphics, Synopsys and Cadence.
A hands-on introduction to FPGA prototyping and SoC design This is the successor edition of the popular FPGA Prototyping by Verilog Examples text. It follows the same “learning-by-doing” approach to teach the fundamentals and practices of HDL synthesis and FPGA prototyping. The new edition uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow the strict design guidelines and coding practices used for large, complex digital systems. The book is completely updated and uses the SystemVerilog language, which “absorbs” the Verilog language. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The new edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelope generator. Expands the original video controller into a complete stream based video subsystem that incorporates a video synchronization circuit, a test-pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Provides a detailed discussion on blocking and nonblocking statements and coding styles. Describes basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Presents basic embedded system software

development. Suggests additional modules and peripherals for interesting and challenging projects. FPGA Prototyping by SystemVerilog Examples makes a natural companion text for introductory and advanced digital design courses and embedded system courses. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

In August of 2006, an engineering VP from one of Altera’s customers approached Misha Burich, VP of Engineering at Altera, asking for help in reliably being able to predict the cost, schedule and quality of system designs reliant on FPGA designs. At this time, I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further. As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process, I noted that this problem was not unique to this one customer. The characteristics of the problem are shared by many Corporations that implement designs in FPGAs. The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams. There is a wide range of design experience across the teams. There is no working process for sharing design blocks between engineering teams. As I analyzed the data that I had received from hundreds of customer visits in the past, I noticed that design reuse among engineering teams was a challenge. I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies. Altera had recently solved this problem as part of its own FPGA design software and IP development process.

The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter SystemTM. However, if the reader uses a different EDA tool, that tool’s commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design. It covers the Verilog 2001 and Verilog 2005 RTL design styles, constructs and the optimization at the RTL and synthesis level. The book also covers the logic synthesis, low power, multiple clock domain design concepts and design performance improvement techniques. The book includes 250 design examples/illustrations and 100 exercise questions. This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework. In addition, it will be a hands-on professional reference and a self-study aid for hobbyists.

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

The primary goal of Parametric Modeling with NX 12 is to introduce the aspects of designing with Solid Modeling and Parametric Modeling. This text is intended to be used as a practical training guide for students and professionals. This text uses NX 12 as the modeling tool, and the chapters proceed in a pedagogical fashion to guide you from constructing basic solid models to building intelligent mechanical designs, creating multi-view drawings and assembly models. This text takes a hands-on, exercise-intensive approach to all the important Parametric Modeling techniques and concepts. This textbook contains a series of fourteen tutorial style lessons designed to introduce beginning CAD users to NX. This text is also helpful to NX users upgrading from a previous release of the software. The solid modeling techniques and concepts discussed in this text are also applicable to other parametric feature-based CAD packages. The basic premise of this book is that the more designs you create using NX, the better you learn the software. With this in mind, each lesson introduces a new set of commands and concepts, building on previous lessons. This book does not attempt to cover all of NX’s features, only to provide an introduction to the software. It is intended to help you establish a good basis for exploring and growing in the exciting field of Computer Aided Engineering. This book also introduces you to the general principles of 3D printing including a brief history of 3D printing, the types of 3D printing technologies, commonly used filaments, and the basic procedure for printing a 3D model. 3D printing makes it easier than ever for anyone to start turning their designs into physical objects, and by the end of this book you will be ready to start printing out your own designs.

Parametric Modeling with Autodesk Inventor 2021 contains a series of seventeen tutorial style lessons designed to introduce Autodesk Inventor, solid modeling, and parametric modeling. It uses a hands-on, exercise-intensive approach to all the important parametric modeling techniques and concepts. The lessons guide the user from constructing basic shapes to building intelligent mechanical designs, to creating multi-view drawings and assembly models. Other featured topics include sheet metal design, motion analysis, 2D design reuse, collision and contact, stress analysis, 3D printing and the Autodesk Inventor 2021 Certified User Examination. Video Training Included with every new copy of this book is access to extensive video training. The video training parallels the exercises found in the text and are designed to be watched first before following the instructions in the book. However, the videos do more than just provide you with click by click instructions. Author Luke Jumper also includes a brief

discussion of each tool, as well as rich insight into why and how the tools are used. Luke isn't just telling you what to do, he's showing and explaining to you how to go through the exercises while providing clear descriptions of the entire process. It's like having him there guiding you through the book. These videos will provide you with a wealth of information and brings the text to life. They are also an invaluable resource for people who learn best through a visual experience. These videos deliver a comprehensive overview of the tools found in Autodesk Inventor and perfectly complement and reinforce the exercises in the book. Autodesk Inventor 2021 Certified User Examination The content of Parametric Modeling with Autodesk Inventor 2021 covers the performance tasks that have been identified by Autodesk as being included on the Autodesk Inventor 2021 Certified User examination. Special reference guides show students where the performance tasks are covered in the book.

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

The primary goal of Parametric Modeling with Creo Parametric 5.0 is to introduce the aspects of Solid Modeling and Parametric Modeling. This text is intended to be used as a training guide for any student or professional wanting to learn to use Creo Parametric. This text covers Creo Parametric and the lessons proceed in a pedagogical fashion to guide you from constructing basic shapes to building intelligent solid models and creating multi-view drawings. This text takes a hands-on, exercise-intensive approach to all the important Parametric Modeling techniques and concepts. This textbook contains a series of eleven tutorial style lessons designed to introduce beginning CAD users to Creo Parametric. The basic premise of this book is that the more designs you create using Creo Parametric, the better you learn the software. With this in mind, each lesson introduces a new set of commands and concepts, building on previous lessons. This book will provide you with a good basis for exploring and growing in the exciting field of Computer Aided Engineering. This book also introduces you to the general principles of 3D printing including a brief history of 3D printing, the types of 3D printing technologies, commonly used filaments, and the basic procedure for printing a 3D model. 3D printing makes it easier than ever for anyone to start turning their designs into physical objects and by the end of this book you will be ready to start printing out your own designs.

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

Conventional computational methods, and even the latest soft computing paradigms, often fall short in their ability to offer solutions to many real-world problems due to uncertainty, imprecision, and circumstantial data. Hybrid intelligent computing is a paradigm that addresses these issues to a considerable extent. The Handbook of Research on Advanced Hybrid Intelligent Techniques and Applications highlights the latest research on various issues relating to the hybridization of artificial intelligence, practical applications, and best methods for implementation. Focusing on key interdisciplinary computational intelligence research dealing with soft computing techniques, pattern mining, data analysis, and computer vision, this book is relevant to the research needs of academics, IT specialists, and graduate-level students.

The primary goal of Parametric Modeling with Pro/ENGINEER Wildfire 5.0 is to introduce the aspects of solid modeling and parametric modeling. The text is a hands-on, exercise-intensive approach to all the important parametric modeling techniques and concepts. This book contains a series of eleven tutorial style lessons designed to introduce beginning CAD users to the most commonly used features of Pro/ENGINEER. Each lesson introduces a new set of commands and concepts, building on previous lessons. This text guides you from constructing basic shapes to building intelligent solid models and creating multi-view drawings. The basic premise of this book is that the more designs you create, the better you learn the software. This book will establish a good basis for exploring and growing in the exciting field of computer aided engineering. By the end of this book the reader will advance to an intermediate level Pro/ENGINEER user.

This book describes RTL design, synthesis, and timing closure strategies for SOC blocks. It covers high-level RTL design scenarios and challenges for SOC design. The book gives practical information on the issues in SOC and ASIC prototyping using modern high-density FPGAs. The book covers SOC performance improvement techniques, testing, and system-level verification. The book also describes the modern Xilinx FPGA architecture and their use in SOC prototyping. The book covers the Synopsys DC, PT commands, and use of them to constraint and to optimize SOC design. The contents of this book will be of use to students, professionals, and hobbyists alike.

Are you have a problem with Synopsys Design Constraints (SDC) or Altera Timing Analyzer? This book will have all the answers for you. It explains about each frequently-used SDC command, specify timing and other design constraints. With Altera time analyzer uses industrystandard constraint and analysis methodology to report on all data required times, data arrival times, and clock arrival times for all register-to-register.

Parametric Modeling with Autodesk Fusion 360 contains a series of thirteen tutorial style lessons designed to introduce Autodesk Fusion 360, solid modeling and parametric modeling techniques and concepts. This book introduces Autodesk Fusion 360 on a step-by-step basis, starting with constructing basic shapes, all the way through to the creation of assembly drawings and 3D printing your own designs. This book takes a hands on, exercise intensive approach to all the important parametric modeling techniques and concepts. Each lesson introduces a new set of commands and concepts, building on previous lessons. The lessons guide you from constructing basic shapes to building intelligent solid models, assemblies and creating multi-view drawings. This book also introduces you to the general principles of 3D printing including a brief history of 3D printing, the types of 3D printing technologies, commonly used filaments, and the basic procedure for printing a

3D model. 3D printing makes it easier than ever for anyone to start turning their designs into physical objects, and by the end of this book you will be ready to start printing out your own designs. Spring 2021 Edition Autodesk Fusion 360 is an entirely cloud based CAD, CAM, and CAE platform that is constantly evolving. This edition of Parametric Modeling with Autodesk Fusion 360 was written using Autodesk Fusion 360 in March of 2021. Fusion 360 is a stable product and all the major tools and features of Fusion 360 used in this edition should continue to operate the same way for the foreseeable future. SDC Publications is committed to updating this book on a regular interval to incorporate new features and changes made to the software. Should a major change to Autodesk Fusion 360 require a newer edition be made available sooner, we will publish a new edition as soon as possible. Older editions will stop being available once newer editions are released.
SOLIDWORKS 2020 Quick Start introduces new users to the basics of using SOLIDWORKS 3D CAD software in five easy lessons. This book is intended for the student or designer who needs to learn SOLIDWORKS quickly and effectively. This book is perfect for engineers in industry who are expected to have SOLIDWORKS skills for their company's next project or students who need to learn SOLIDWORKS without taking a comprehensive CAD course. Based on years of teaching SOLIDWORKS to engineering students, SOLIDWORKS 2020 Quick Start concentrates on the areas where new users can improve efficiency in the design modeling process. By learning the correct SOLIDWORKS skills and file management techniques, you gain the most knowledge in the shortest period of time. This book begins with an overview of SOLIDWORKS and the User Interface (UI), its menus, toolbars and commands. With a quick pace, you learn the essentials of 2D sketching, part and assembly creation, perform motion study, develop detailed part and assembly drawings and much more. Throughout this book you develop a mini Stirling Engine and investigate the proper design intent and constraints.
A hands-on introduction to FPGA prototyping and SoC design This Second Edition of the popular book follows the same "learning-by-doing" approach to teach the fundamentals and practices of VHDL synthesis and FPGA prototyping. It uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow strict design guidelines and coding practices used for large, complex digital systems. The new edition is completely updated. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software "programmability" and develop complex and interesting embedded system projects. The revised edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelop generator. Expands the original video controller into a complete stream-based video subsystem that incorporates a video synchronization circuit, a test pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Introduces basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Introduces basic embedded system software development. Suggests additional modules and peripherals for interesting and challenging projects. The FPGA Prototyping by VHDL Examples, Second Edition makes a natural companion text for introductory and advanced digital design courses and embedded system course. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.