Clock Domain Crossing University Of Florida

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

This book describes an approach for designing Systems-on-Chip such that the system meets precise mathematical requirements. The methodologies presented enable embedded systems designers to reuse intellectual property (IP) blocks from existing designs in an efficient, reliable manner, automatically generating correct SoCs from multiple, possibly mismatching, components.

Principles of Asynchronous Circuit Design - A Systems Perspective addresses the need for an introductory text on asynchronous circuit design. Part I is an 8-chapter tutorial which addresses the most important issues for the beginner, including how to think about asynchronous systems. Part II is a 4-chapter introduction to Balsa, a freely-available synthesis system for asynchronous circuits which will enable the reader to get hands-on experience of designing high-level asynchronous systems. Part III offers a number of examples of state-of-the-art asynchronous systems to illustrate what can be built using asynchronous techniques. The examples range from a complete commercial smart card chip to complex microprocessors. The objective in writing this book has been to enable industrial designers with a background in conventional (clocked) design to be able to understand asynchronous design sufficiently to assess what it has to offer and whether it might be advantageous in their next design task.

This book presents the state of the art in high-performance computing and simulation on modern supercomputer architectures. It covers trends in hardware and software development in general and the future of high-performance systems and heterogeneous architectures in particular. The application-related contributions cover computational fluid dynamics, material science, medical applications and climate research; innovative fields such as coupled multi-physics and multi-scale simulations are highlighted. All papers were chosen from presentations given at the 18th Workshop on Sustained Simulation Performance held at the HLRS, University of Stuttgart, Germany in October 2013 and subsequent Workshop of the same name held at Tohoku University in March 2014.

"Tom is not prepared for what is about to happen when he hears the grandfather clock strike thirteen. Outside the back door is a garden, which everyone tells him does not exist."--Page 4 de la couverture.

Create low power, higher performance circuits with shorter design times using this practical guide to asynchronous design. This practical alternative to conventional synchronous design enables performance close to full-custom designs with design times that approach commercially available ASIC standard cell flows. It includes design trade-offs, specific design examples, and end-of-chapter exercises. Emphasis throughout is placed on practical techniques and real-world applications, making this ideal for circuit design students interested in alternative design styles and system-on-chip circuits, as well as circuit designers in industry who need new solutions to old problems.

A journey through a land where Milo learns the importance of words and numbers provides a cure for his boredom.

What makes some computers slow? Why do some digital systems operate reliably for years while others fail mysteriously every few hours? How can some systems dissipate kilowatts while others operate off batteries? These questions of speed, reliability, and power are all determined by the system-level electrical design of a digital system. Digital Systems Engineering presents a comprehensive treatment of these topics. It combines a rigorous development of the fundamental principles in each area with real-world examples of circuits and methods. The book not only serves as an undergraduate textbook, filling the gap between circuit design and logic design, but can also help practising digital designers keep pace with the speed and power of modern integrated circuits. The techniques described in this book, once used only in supercomputers, are essential to the correct and efficient operation of any type of digital system.

This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2004, held in Santorini, Greece in September 2004. The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted. The papers are organized in topical sections on buses and communication, circuits and devices, low power issues, architectures, asynchronous circuits, systems design, interconnect and physical design, security and safety, low-power processing, digital design, and modeling and simulation.

The SAMOS workshop is an international gathering of highly quali?ed researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly)

unsolved problems and in-depth topical reviews can be unleashed in the sci- ti?c arena. Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I–IV (2001–2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), T- wan (1), Turkey (2), UK (2), and USA (5). We are grateful to all of the authors who submitted papers to the workshop.

Today’s networks of processors on and off chip, operating with independent clocks, need effective synchronization of the data passing between them for reliability. When two or more processors request access to a common resource, such as a memory, an arbiter has to decide which request to deal with first. Current developments in integrated circuit processing are leading to an increase in the numbers of independent digital processing elements in a single system. With this comes faster communications, more networks on chip, and the demand for more reliable, more complex, and higher performance synchronizers and arbiters. Written by one of the foremost researchers in this area of digital design, this authoritative text provides in-depth theory and practical design solutions for the reliable working of synchronization and arbitration hardware in digital systems. The book provides methods for making real reliability measurements both on and off chip, evaluating some of the common difficulties and detailing circuit solutions at both circuit and system levels. Synchronization and Arbitration in Digital Systems also presents: mathematical models used to estimate mean time between failures in digital systems; a summary of serial and parallel communication techniques for on-chip data transmission; explanations on how to design a wrapper for a locally synchronous cell, highlighting the issues associated with stoppable clocks; an examination of various types of priority arbiters, using signal transition graphs to show the specification of different designs (from the simplest to more complex multi-way arbiters) including ways of solving problems encountered in a wide range of applications; essential information on systems composed of independently timed regions, including a discussion on the problem of choice and the factors affecting the time taken to make choices in electronics. With its logical approach to design methodology, this will prove an invaluable guide for electronic and computer engineers and researchers working on the design of digital electronic hardware. Postgraduates and senior undergraduate students studying digital systems design as part of their electronic engineering course will struggle to find a resource that better details the information given inside this book

This Expert Guide gives you the techniques and technologies in digital signal processing (DSP) to optimally design and implement your embedded system. Written by experts with a solutions focus, this encyclopedic reference gives you an indispensable aid to tackling the day-to-day problems you face in using DSP to develop embedded systems. With this book you will learn: A range of development techniques for developing DSP code Valuable tips and tricks for optimizing DSP software for maximum performance The various options available for constructing DSP systems from numerous software components The tools available for developing DSP applications Numerous practical guidelines from experts with wide and lengthy experience of DSP application development Features: Several areas of research being done in advanced DSP technology Industry case studies on DSP systems development DSP for Embedded and Real-Time Systems is the reference for both the beginner and experienced, covering most aspects of using today’s DSP techniques and technologies for designing and implementing an optimal embedded system. The only complete reference which explains all aspects of using DSP in embedded systems development making it a rich resource for every day use Covers all aspects of using today’s DSP techniques and technologies for designing and implementing an optimal embedded system Enables the engineer to find solutions to all the problems they will face when using DSP

This book contains extended and revised versions of the best papers presented at the 24th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2016, held in Tallinn, Estonia, in September 2016. The 11 papers included in the book were carefully reviewed and selected from the 36 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the latest scientific and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) Design.

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.

"Information security covers the protection of information against unauthorized disclosure, transfer, modification, and destruction, whether accidentally or intentionally. Quality of life in general and of individual citizens, and the effectiveness of the economy critically depends on our ability to build software in a transparent and efficient way. Furthermore, we must be able to enhance the software development process systematically in order to ensure software's safety and security. This, in turn, requires very high software reliability, i.e., an extremely high confidence in the ability of the software to perform flawlessly. Foundations of software technology provide models that enable us to capture application domains and their requirements, but also to understand the structure and working of software systems and software architectures. Based on these foundations tools allow to prove and ensure the correctness of software's functioning. New developments must pay due diligence to the importance of security-related aspects, and align current methods and techniques to information security, integrity, and system reliability. The articles in this book describe the state-of-the-art ideas on how to meet these challenges in software engineering."

Since register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.

This book shares with readers practical design knowledge gained from the author's 24 years of IC design experience. The author addresses issues and challenges faced commonly by IC designers, along with solutions and workarounds. Guidelines are described for tackling issues such as clock domain crossing, using lockup latch to cross clock domains during scan shift, implementation of scan chains across power domain, optimization methods to improve timing, how standard cell libraries can aid in synthesis optimization, BKM (best known method) for RTL coding, test compression, memory BIST, usage of signed Verilog for design requiring +ve and -ve calculations, state machine, code coverage and much more. Numerous figures and examples are provided to aid the reader in understanding the issues and their workarounds.

This book highlights the complex issues, tasks and skills that must be mastered by an IP designer, in order to design an optimized and robust digital circuit to solve a problem. The techniques and methodologies described can serve as a bridge between specifications that are known to the designer and RTL code that is final outcome, reducing significantly the time it takes to convert initial ideas and concepts into right-first-time silicon. Coverage focuses on real problems rather than theoretical concepts, with an emphasis on design techniques across various aspects of chip-design.

This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

"IEEE Computer Society Order Number P2133"--T.p. verso.

Provides students with a system-level perspective and the tools they need to understand, analyze and design complete digital systems using Verilog. It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems, reflecting digital design in the real world.

To cope with the new running conditions in the ALICE experiment at the Large Hadron Collider at CERN, a new integrated circuit named SAMPA has been created that can process 32 analogue channels, convert them to digital, perform filtering and compression, and transmit the data on high speed links to the data acquisition system. The main purpose of this work is to specify, design, test and verify the digital signal processing part of the SAMPA device to accommodate the requirements of the detectors involved. Innovative solutions have been employed to reduce the bandwidth required by the detectors, as well as adaptations to ease data handling later in the processing chain. The new SAMPA device was built to replace two existing circuits, in addition to reducing the current consumption, and doubling the amount of processing channels. About 50000 of the devices will be installed in the Time Projection Chamber and Muon Chamber detectors in the ALICE experiment.

The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient,portable, and scalable Register Transfer Level (RTL) digitalcircuits using the VHDL hardware description language and synthesissoftware. Focusing on the module-level design, which is composed offunctional units, routing circuit, and storage, the bookillustrates the relationship between the VHDL constructs and theunderlying hardware components, and shows how to develop codes thatfaithfully reflect the module-level design and can be synthesizedinto efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDLconstructs and hardware components * Conceptual diagrams that illustrate the realization of VHDLcodes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce designconcepts,

procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs andcoding * One chapter covering the synchronization and interface betweenmultiple clock domains Although the focus of the book is RTL synthesis, it also examinesthe synthesis task from the perspective of the overall developmentprocess. Readers learn good design practices and guidelines toensure that an RTL design can accommodate future simulation,verification, and testing needs, and can be easily incorporatedinto a larger system or reused. Discussion is independent oftechnology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practicalexamples, this is an excellent textbook for upper-levelundergraduate or graduate courses in advanced digital logic.Engineers who need to make effective use of today's synthesissoftware and FPGA devices should also refer to this book.

Design and Verification of Clock Domain Crossing InterfacesA Digital Signal Processor for Particle DetectorsDesign, Verification and TestingSpringer Nature

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This book brings together a selection of the best papers from the eighteenth edition of the Forum on specification and Design Languages Conference (FDL), which took place on September 14-16, 2015, in Barcelona, Spain. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems.

This book constitutes the refereed proceedings of the 5th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2005, held in Samos, Greece in July 2005. The 49 revised full papers presented were thoroughly reviewed and selected from 114 submissions. The papers are organized in topical sections on reconfigurable system design and implementations, processor architectures, design and simulation, architectures and implementations, system level design, and modeling and simulation.

As Moore’s law continues to unfold, two important trends have recently emerged. First, the growth of chip capacity is translated into a corresponding increase of number of cores. Second, the parallelization of the computation and 3D integration technologies lead to distributed memory architectures. This book describes recent research that addresses urgent challenges in many-core architectures and application mapping. It addresses the architectural design of many core chips, memory and data management, power management, design and programming methodologies. It also describes how new techniques have been applied in various industrial case studies.

mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

This monograph is based on the third author's lectures on computer architecture, given in the summer semester 2013 at Saarland University, Germany. It contains a gate level construction of a multi-core machine with pipelined MIPS processor cores and a sequentially consistent shared memory. The book contains the first correctness proofs for both the gate level implementation of a multi-core processor and also of a cache based sequentially consistent shared memory. This opens the way to the formal verification of synthesizable hardware for multi-core processors in the future. Constructions are in a gate level hardware model and thus deterministic. In contrast the reference models against which correctness is shown are nondeterministic. The development of the additional machinery for these proofs and the correctness proof of the shared memory at the gate level are the main technical contributions of this work.

This book constitutes the thoroughly refereed joint post-proceedings of the two International Workshops on Formal Methods for Industrial Critical Systems, FMICS 2006, and on Parallel and Distributed Methods in Verification, PDMC 2006, held in Bonn, Germany in August 2006 in the course of the 17th International Conference on Concurrency Theory, CONCUR 2006.