A Structured Vhdl Design Method Gaisler

Compendio de los trabajos presentados en Toledo durante el VHDL user's forum in Europe.

This book constitutes the refereed proceedings of the Second International Conference on the Unified Modeling Language, UML'99, held in Fort Collins, CO, USA in September 1999. The 44 revised full papers presented together with two invited contributions and three panel summaries were carefully reviewed and selected from a total of 166 submissions. The papers are organized in topical sections on software architecture, UML and other notations, formalizing interactions, meta modeling, tools, components, UML extension mechanisms, process modeling, real-time systems, constraint languages, analyzing UML models, precise behavioral modeling, applying UML sequence design, and coding.

IJCNN '99 spans the neural network field from neurons to consciousness, training algorithms to robotics, chaos to control, fuzzy logic to evolutionary computing. Starting with a symposium on biological neural networks, it explores the potential impact of neurobiological discoveries.

The Sixth International Conference on Reliable Software Technologies, Ada- Europe 2001, took place in Leuven, Belgium, May 14-18, 2001. It was

sponsored by Ada-Europe, the European federation of national Ada societies, in cooperation with ACM SIGAda, and it was organized by members of the K.U. Leuven and Ada- Belgium. This was the 21st consecutive year of Ada-Europe conferences and the sixth year of the conference focusing on the area of reliable software technologies. The use of software components in embedded systems is almost ubiquitous: planes fly by wire, train signalling systems are now computer based, mobile phones are digital devices, and biological, chemical, and manufacturing plants are controlled by software, to name only a few examples. Also other, non-embedded, mission-critical systems depend more and more upon software. For these products and processes, reliability is a key success factor, and often a safety-critical hard requirement. It is well known and has often been experienced that quality cannot be added to software as a mere afterthought. This also holds for reliability. Moreover, the reliability of a system is not due to and cannot be built upon a single technology. A wide range of approaches is needed, the most difficult issue being their purposeful integration. Goals of reliability must be precisely defined and included in the requirements, the development process must be controlled to achieve these goals, and sound development methods must be used to fulfill these non-functional requirements.

This book reviews fault-tolerance techniques for SRAM-based Field Programmable Gate Arrays (FPGAs), outlining many methods for designing fault tolerance systems. Some of these are based on new fault-tolerant architecture, and others on protecting the high-level hardware description before synthesis in the FPGA. The text helps the reader choose the best techniques project-by-project, and to compare fault tolerant techniques for programmable logic applications.

Embedded systems are usually composed of several interacting components such as custom or application specific processors, ASICs, memory blocks, and the associated communication infrastructure. The development of tools to support the design of such systems requires a further step from high-level synthesis towards a higher abstraction level. The lack of design tools accepting a system-level specification of a complete system, which may include both hardware and software components, is one of the major bottlenecks in the design of embedded systems. Thus, more and more research efforts have been spent on issues related to system-level synthesis. This book addresses the two most active research areas of design automation today: high-level synthesis and system-level synthesis. In particular, a transformational approach to synthesis from VHDL specifications is described. System Synthesis with VHDL provides a coherent

view of system synthesis which includes the high-level and the system-level synthesis tasks. VHDL is used as a specification language and several issues concerning the use of VHDL for high-level and system-level synthesis are discussed. These include aspects from the compilation of VHDL into an internal design representation to the synthesis of systems specified as interacting VHDL processes. The book emphasizes the use of a transformational approach to system synthesis. A Petri net based design representation is rigorously defined and used throughout the book as a basic vehicle for illustration of transformations and other design concepts. Iterative improvement heuristics, such as tabu search, simulated annealing and genetic algorithms, are discussed and illustrated as strategies which are used to guide the optimization process in a transformation-based design environment. Advanced topics, including hardware/software partitioning, test synthesis and low power synthesis are discussed from the perspective of a transformational approach to system synthesis. System Synthesis with VHDL can be used for advanced undergraduate or graduate courses in the area of design automation and, more specifically, of high-level and system-level synthesis. At the same time the book is intended for CAD developers and researchers as well as industrial designers of digital systems who are interested in new algorithms and techniques

supporting modern design tools and methodologies. Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The first volume, EDA for IC System Design, Verification, and Testing, thoroughly examines system-level design, microarchitectural design, logical verification, and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools, using performance metrics to select microprocessor cores for IC designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. Save on the complete set.

Are you an RTL or system designer that is currently using, moving, or planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along

with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.

This three-volume set constitutes the refereed proceedings of the International Conference on Computational Science and its Applications. These volumes feature outstanding papers that present a wealth of original research results in the field of computational science, from foundational issues in computer science and mathematics to advanced applications in almost all sciences that use computational techniques.

This book introduces a modern approach to embedded system design, presenting software design and hardware design in a unified manner. It covers trends and challenges, introduces the design

and use of single-purpose processors ("hardware") and general-purpose processors ("software"), describes memories and buses, illustrates hardware/software tradeoffs using a digital camera example, and discusses advanced computation models, controls systems, chip technologies, and modern design tools. For courses found in EE, CS and other engineering departments.

A guide to applying software design principles and coding practices to VHDL to improve the readability, maintainability, and quality of VHDL code. This book addresses an often-neglected aspect of the creation of VHDL designs. A VHDL description is also source code, and VHDL designers can use the best practices of software development to write high-quality code and to organize it in a design. This book presents this unique set of skills, teaching VHDL designers of all experience levels how to apply the best design principles and coding practices from the software world to the world of hardware. The concepts introduced here will help readers write code that is easier to understand and more likely to be correct, with improved readability, maintainability, and overall quality. After a brief review of VHDL, the book presents fundamental design principles for writing code, discussing such topics as design, quality, architecture, modularity, abstraction, and hierarchy. Building on these concepts, the book then introduces and provides recommendations for each

basic element of VHDL code, including statements, design units, types, data objects, and subprograms. The book covers naming data objects and functions, commenting the source code, and visually presenting the code on the screen. All recommendations are supported by detailed rationales. Finally, the book explores two uses of VHDL: synthesis and testbenches. It examines the key characteristics of code intended for synthesis (distinguishing it from code meant for simulation) and then demonstrates the design and implementation of testbenches with a series of examples that verify different kinds of models, including combinational, sequential, and FSM code. Examples from the book are also available on a companion website, enabling the reader to experiment with the complete source code.

Models in system design follow the general tendency in electronics in terms of size, complexity and difficulty of maintenance. While a model should be a manageable representation of a system, this increasing complexity sometimes forces current CAD-tool designers and model writers to apply modeling techniques to the model itself. Model writers are interested in instrumenting their model, so as to extract critical information before the model is complete. CAD tools designers use internal representations of the design at various stages. The complexity has also led CAD-tool developers to

develop formal tools, theories and methods to improve relevance, completeness and consistency of those internal representations. Information modeling involves the representation of objects, their properties and relationships. Performance Modeling When it comes to design choices and trade-offs, performance is generally the final key. However performance estimations have to be extracted at a very early stage in the system design. Performance modeling concerns the set of tools and techniques that allow or help the designer to capture metrics relating to future architectures. Performance modeling encompasses the whole system, including software modeling. It has a strong impact on all levels of design choices, from hardware/software partitioning to the final layout. Information Modeling Specification and formalism have in the past traditionally played little part in the design and development of EDA systems, their support environments, languages and processes. Instead, EDA system developers and EDA system users have seemed to be content to operate within environments that are often extremely complex and may be poorly tested and understood. This situation has now begun to change with the increasing use of techniques drawn from the domains of formal specification and database design. This section of this volume addresses aspects of the techniques being used. In particular, it considers a specific

formalism, called information modeling, which has gained increasing acceptance recently and is now a key part of many of the proposals in the EDA Standards Roadmap, which promises to be of significance to the EDA industry. In addition, the section looks at an example of a design system from the point of view of its underlying understanding of the design process rather than through a consideration of particular CAD algorithms. Meta-Modeling: Performance and Information Modeling contains papers describing the very latest techniques used in meta-modeling. It will be a valuable text for researchers, practitioners and students involved in Electronic Design Automation. The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient,portable, and scalable Register Transfer Level (RTL) digitalcircuits using the VHDL hardware description language and synthesissoftware. Focusing on the module-level design, which is composed offunctional units, routing circuit, and storage, the bookillustrates the relationship between the VHDL constructs and theunderlying hardware components, and shows how to develop codes thatfaithfully reflect the module-level design and can be synthesizedinto efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDLconstructs

and hardware components * Conceptual diagrams that illustrate the realization of VHDLcodes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce designconcepts, procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs andcoding * One chapter covering the synchronization and interface betweenmultiple clock domains Although the focus of the book is RTL synthesis, it also examinesthe synthesis task from the perspective of the overall developmentprocess. Readers learn good design practices and guidelines toensure that an RTL design can accommodate future simulation,verification, and testing needs, and can be easily incorporatedinto a larger system or reused. Discussion is independent oftechnology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practicalexamples, this is an excellent textbook for upper-levelundergraduate or graduate courses in advanced digital logic.Engineers who need to make effective use of today's synthesissoftware and FPGA devices should also refer to this book.

* Teaches VHDL by example * Includes tools for simulation and synthesis * CD-ROM containing Code/Design examples and a working demo of ModelSIM

Languages, Design Methods, and Tools for Electronic System

DesignSelected Contributions from FDL 2013Springer
This book will show you how to approach the design covering everything from the circuit specification to the final design acceptance, including what support you can expect, sizing, timing analysis, power and packaging, various simulations, design verification, and design submission.
The success of VHDL since it has been balloted in 1987 as an IEEE standard may look incomprehensible to the large population of hardware designers, who had never heared of Hardware Description Languages before (for at least 90% of them), as well as to the few hundreds of specialists who had been working on these languages for a long time (25 years for some of them). Until 1988, only a very small subset of designers, in a few large companies, were used to describe their designs using a proprietary HDL, or sometimes a HDL inherited from a University when some software environment happened to be developped around it, allowing usability by third parties. A number of benefits were definitely recognized to this practice, such as functional verification of a specification through simulation, first performance evaluation of a tentative design, and sometimes automatic microprogram generation or even automatic high level synthesis. As there was apparently no market for HDL's, the ECAD vendors did not care about them, start-up companies were seldom able to survive in this area, and large users of proprietary tools were spending more and more people and money just to maintain their internal system.
Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer. As a result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now

available. These designers see current design tools and methodologies as inadequate for developing million-gate ASICs from scratch. There is considerable pressure to keep design team size and design schedules constant even as design complexities grow. Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology. Design reuse - the use of pre-designed and pre-verified cores - is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a coherent, integrated view of the design process. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high-quality SoC designs.

Annotation This is a two-volume set of the proceedings of the September 1999 conference on the current and future developments in informatics theories and application areas. Volume I (80 contributions) discusses digital system design, architectures, and methods and tools. Volume II (30 contributions) covers music technology and audio processing, dependable computing systems, software process and product improvement, multimedia and telecommunication, and network computing. Lacks a subject index. Annotation copyrighted by Book News, Inc., Portland, OR.

In the past few decades Computer Hardware Description

Languages (CHDLs) have been a rapidly expanding subject area due to a number of factors, including the advancing complexity of digital electronics, the increasing prevalence of generic and programmable components of software-hardware and the migration of VLSI design to high level synthesis based on HDLs. Currently the subject has reached the consolidation phase in which languages and standards are being increasingly used, at the same time as the scope is being broadened to additional application areas. This book presents the latest developments in this area and provides a forum from which readers can learn from the past and look forward to what the future holds.

This book brings together a selection of the best papers from the sixteenth edition of the Forum on specification and Design Languages Conference (FDL), which was held in September 2013 in Paris, France. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems and mixed-technology systems.

Masters Theses in the Pure and Applied Sciences was first conceived, published, and disseminated by the Center for Information and Numerical Data Analysis and Synthesis (CINDAS)* at Purdue University in 1957, starting its coverage of theses with the academic year 1955. Beginning with Volume 13, the printing and dis semination phases of the activity were transferred to University Microfilms/Xerox of Ann Arbor, Michigan, with the though that such an arrangement would be more

beneficial to the academic and general scientific and technical community. After five years of this joint undertaking we had concluded that it was in the interest of all concerned if the printing and distribution of the volumes were handled by an international publishing house to assure improved service and broader dissemi nation. Hence, starting with Volume 18, Masters Theses in the Pure and Applied Sciences has been disseminated on a worldwide basis by Plenum Publishing Corporation of New York, and in the same year the coverage was broadened to include Canadian universities. All back issues can also be ordered from Plenum. We have reported in Volume 37 (thesis year 1992) a total of 12,549 thesis titles from 25 Canadian and 153 United States universities. We are sure that this broader base for these titles reported will greatly enhance the value of this impor tant annual reference work. While Volume 37 reports theses submitted in 1992, on occasion, certain uni versities do report theses submitted in previous years but not reported at the time.

This book brings together a selection of the best papers from the seventeenth edition of the Forum on specification and Design Languages Conference (FDL), which took place on October 14-16, 2014, in Munich, Germany. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new

ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems.

Two large international conferences on Advances in Engineering Sciences were held in Hong Kong, March 18–20, 2015, under the International MultiConference of Engineers and Computer Scientists (IMECS 2015), and in London, UK, 1–3 July, 2015, under the World Congress on Engineering (WCE 2015) respectively. This volume contains 35 revised and extended research articles written by prominent researchers participating in the conferences. Topics covered include engineering mathematics, computer science, electrical engineering, manufacturing engineering, industrial engineering, and industrial applications. The book offers state-of-the-art advances in engineering sciences and also serves as an excellent reference work for researchers and graduate students working with/on engineering sciences.

As electronic technology reaches the point where complex systems can be integrated on a single chip, and higher degrees of performance can be achieved at lower costs, designers must devise new ways to undertake the laborious task of coping with the numerous, and non-trivial, problems that arise during the conception of such systems. On the other hand,

shorter design cycles (so that electronic products can fit into shrinking market windows) put companies, and consequently designers, under pressure in a race to obtain reliable products in the minimum period of time. New methodologies, supported by automation and abstraction, have appeared which have been crucial in making it possible for system designers to take over the traditional electronic design process and embedded systems is one of the fields that these methodologies are mainly targeting. The inherent complexity of these systems, with hardware and software components that usually execute concurrently, and the very tight cost and performance constraints, make them specially suitable to introduce higher levels of abstraction and automation, so as to allow the designer to better tackle the many problems that appear during their design. Advanced Techniques for Embedded Systems Design and Test is a comprehensive book presenting recent developments in methodologies and tools for the specification, synthesis, verification, and test of embedded systems, characterized by the use of high-level languages as a road to productivity. Each specific part of the design process, from specification through to test, is looked at with a constant emphasis on behavioral methodologies. Advanced Techniques for Embedded Systems Design and Test is essential reading for all researchers in the design

and test communities as well as system designers and CAD tools developers.

Embedded systems have been almost invisibly pervading our daily lives for several decades. They facilitate smooth operations in avionics, automotive electronics, or telecommunication. New problems arise by the increasing employment, interconnection, and communication of embedded systems in heterogeneous environments: How secure are these embedded systems against attacks or breakdowns? Therefore, how can embedded systems be designed to be more secure? How can embedded systems autonomically react to threats? Facing these questions, Sorin A. Huss is significantly involved in the exploration of design methodologies for secure embedded systems. This Festschrift is dedicated to him and his research on the occasion of his 60th birthday.

This book represents an attempt to treat three aspects of digital systems, design, prototyping and customization, in an integrated manner using two major technologies: VHSIC Hardware Description Language (VHDL) as a modeling and specification tool, and Field-Programmable Logic Devices (FPLDs) as an implementation technology. They together make a very powerful combination for complex digital systems rapid design and prototyping as the important steps towards manufacturing, or, in the case of feasible quantities, they also provide fast

system manufacturing. Combining these two technologies makes possible implementation of very complex digital systems at the desk. VHDL has become a standard tool to capture features of digital systems in a form of behavioral, dataflow or structural models providing a high degree of flexibility. When augmented by a good simulator, VHDL enables extensive verification of features of the system under design, reducing uncertainties at the latter phases of design process. As such, it becomes an unavoidable modeling tool to model digital systems at various levels of abstraction.

Lists citations with abstracts for aerospace related reports obtained from world wide sources and announces documents that have recently been entered into the NASA Scientific and Technical Information Database.

The Student's Guide to VHDL is a condensed edition of The Designer's Guide to VHDL, the most widely used textbook on VHDL for digital system modeling. The Student's Guide is targeted as a supplemental reference book for computer organization and digital design courses. Since publication of the first edition of The Student's Guide, the IEEE VHDL and related standards have been revised. The Designer's Guide has been revised to reflect the changes, so it is appropriate that The Student's Guide also be revised. In The Student's Guide to VHDL, 2nd Edition, we have included a design case study illustrating an FPGA-based design flow. The aim is to show how VHDL modeling fits into a design

flow, starting from high-level design and proceeding through detailed design and verification, synthesis, FPGA place and route, and final timing verification. Inclusion of the case study helps to better serve the educational market. Currently, most college courses do not formally address the details of design flow. Students may be given informal guidance on how to proceed with lab projects. In many cases, it is left to students to work it out for themselves. The case study in The Student's Guide provides a reference design flow that can be adapted to a variety of lab projects.

This book gathers selected papers from the Second International Symposium on Software Reliability, Industrial Safety, Cyber Security and Physical Protection of Nuclear Power Plant, held in Chengdu, China on August 23–25, 2017. The symposium provided a platform of technical exchange and experience sharing for a broad range of experts, scholars and nuclear power practitioners. The book reflects the state of the art and latest trends in nuclear instrumentation and control system technologies, as well as China’s growing influence in this area. It offers a valuable resource for both practitioners and academics working in the field of nuclear instrumentation, control systems and other safety-critical systems, as well as nuclear power plant managers, public officials and regulatory authorities.

"Unlike other texts on this topic, Dr. Berger's book takes the software developer's point-of-view. Instead of simply demonstrating how to design a computer's hardware, it provides an understanding of the total machine, highlighting strengths and weaknesses, explaining how

to deal with memory and how to write efficient assembly code that interacts directly with and takes best advantage of the underlying machine."--Jacket. Improvement in the quality of integrated circuit designs and a designer's productivity can be achieved by a combination of two factors: Using more structured design methodologies for extensive reuse of existing components and subsystems. It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of methodologies and tools. Providing higher level design tools allowing to start from a higher level of abstraction. After the success and the widespread acceptance of logic and RTL synthesis, the next step is behavioral synthesis, commonly called architectural or high-level synthesis. Behavioral Synthesis and Component Reuse with VHDL provides methods and techniques for VHDL based behavioral synthesis and component reuse. The goal is to develop VHDL modeling strategies for emerging behavioral synthesis tools. Special attention is given to structured and modular design methods allowing hierarchical behavioral specification and design reuse. The goal of this book is not to discuss behavioral synthesis in general or to discuss a specific tool but to describe the specific issues related to behavioral synthesis of VHDL description. This book targets designers who have to use behavioral synthesis tools or who wish to discover the real possibilities of this emerging technology. The book will also be of interest to teachers and students interested to learn or to teach VHDL based behavioral synthesis.

The power of VHDL-without the complexity! Want to leverage VHDL's remarkable power without bogging down in its notorious complexity? Get A VHDL Primer, Third Edition. This up-to-the-minute introduction to VHDL focuses on the features you need to get results-with extensive practical examples so you can start writing VHDL models immediately. Written by Jayaram Bhasker, one of the world's leading VHDL course developers, this best-selling guide has been completely updated to reflect the popular IEEE STD_LOGIC_1164 package. With Bhasker's help, you'll master all these key VHDL techniques: Behavioral, dataflow and structural modeling. Generics and configurations. Subprograms and overloading. Packages and libraries. Model simulation. Advanced features: Entity statements, generate statements, aliases, guarded signals, attributes, aggregate targets, and more. The book's extensive hardware modeling coverage includes modeling of regular structures, delays, conditional operations, state machines, Moore and Mealy FSMs, clock dividers and much more. You'll find new coverage of text I/O and test benches, as well as complete listings of the IEEE TD_LOGIC_1164 package. J. Bhasker has helped tens of thousands of professionals master VHDL. With A VHDL Primer, Third Edition, it's your turn to succeed.

The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling – including simulation, verification by correctness proofs, synthesis and test. The strong relationship between the topics of CHDL'91

and the work around the use and re-standardization of the VHDL language is also explored. The quality of this proceedings, and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled.