A Digital Phase Locked Loop Based Signal And Symbol Recovery System For Wireless Channel Signals And Communication Technology

Applications of phase-locked loops play an increasingly important role in modern electronic systems, and the last 25 years have seen new developments in the underlying theories as well. Phase-Locked Loops presents the latest information on the basic theory and applications of PLLs. Organized in a logical format, it first introduces the subject in a qualitative manner and discusses key applications. Next, it develops basic models for components of a PLL, and these are used to develop a basic PLL model. The text then discusses both linear and nonlinear methods that are used to analyze the basic PLL model. This book includes extensive coverage of the nonlinear behavior of phase-locked loops, an important area of this field and one where exciting new research is being performed. No other book available covers this critical area in such careful detail. Improvements brought about by the advent of the personal computer, especially in the use of numerical results, are integrated into the text. This book also focuses on PLL component technologies used in system implementation.

Noise-Shaping All-Digital Phase-Locked LoopsModeling, Simulation, Analysis and DesignSpringer Science & Business Media

Featuring an extensive 40 page tutorial introduction, this carefully compiled anthology of 65 of the most important papers on phase-locked loops and clock recovery circuits brings you comprehensive coverage of the field-all in one self-contained volume. You'll gain an understanding of the analysis, design, simulation, and implementation of phase-locked loops and clock recovery circuits in CMOS and bipolar technologies along with valuable insights into the issues and trade-offs associated with phase locked systems for high speed, low power, and low noise.

A systematic design procedure for a second-order digital phase-locked loop with a linear phase detector is proposed. The design procedure is based on the analogy between a type-II second-order analog PLL and a digital PLL. A new digital PLL architecture featuring a linear phase detector which eliminates the noise-bandwidth tradeoff is presented. It employs a stochastic time-to-digital converter (STDC) and a high frequency delta-sigma dithering to achieve a wide PLL bandwidth and a low jitter. The measured results obtained from the prototype chip demonstrate a significant jitter improvement with the STDC.

Phase Locked Loop frequency synthesis is a key component of all wireless systems. This is a complete toolkit for PLL synthesizer design, with MathCAD, SIMetrix files included on CD, allowing readers to perform sophisticated calculation and simulation exercises. Describes how to calculate PLL performance by using standard mathematical or circuit analysis programs

A new and innovative paradigm for RF frequency synthesis and wireless transmitter design Learn the techniques for designing and implementing an all-digital RF frequency synthesizer. In contrast to traditional RF techniques, this innovative book sets forth digitally intensive design techniques that lead the way to the development of low-cost, low-power, and highly integrated circuits for RF functions in deep submicron CMOS processes. Furthermore, the authors demonstrate how the architecture enables readers to integrate an RF front-end with the digital back-end onto a single silicon die using standard ASIC design flow. Taking a bottom-up approach that progressively builds skills and knowledge, the book begins with an introduction to basic concepts of frequency synthesis and then guides the reader through an all-digital RF frequency synthesizer design: Chapter 2 presents a digitally controlled oscillator (DCO), which is the foundation of a novel architecture, and introduces a time-domain model used for analysis and VHDL simulation Chapter 3 adds a hierarchical layer of arithmetic abstraction to the DCO that makes it easier to operate algorithmically Chapter 4 builds a phase correction mechanism around the DCO such that the system's frequency drift or wander performance matches that of the stable external frequency reference Chapter 5 presents an application of the all-digital RF synthesizer Chapter 6 describes the behavioral modeling and simulation methodology used in design The final chapter presents the implementation of a full transmitter and experimental results. The novel ideas presented here have been implemented and proven in two high-volume, commercial single-chip radios developed at Texas Instruments: Bluetooth and GSM. While the focus of the book is on RF frequency synthesizer design, the techniques can be applied to the design of other digitally assisted analog circuits as well. This book is a must-read for students and engineers who want to learn a new paradigm for RF frequency synthesis and wireless transmitter design using digitally intensive design techniques.

Fundamentals of Digital Logic With VHDL Design teaches the basic design techniques for logic circuits. It emphasizes the synthesis of circuits and explains how circuits are implemented in real chips. Fundamental concepts are illustrated by using small examples, which are easy to understand. Then, a modular approach is used to show how larger circuits are designed. VHDL is used to demonstrate how the basic building blocks and larger systems are defined in a hardware description language, producing designs that can be implemented with modern CAD tools. The book emphasizes the concepts that should be covered in an introductory course on logic design, focusing on: Logic functions, gates, and rules of Boolean algebra Circuit synthesis and optimization techniques Number representation and arithmetic circuits Combinational-circuit building blocks, such as multiplexers, decoders, encoders, and code converters Sequential-circuit building blocks, such as flip-flops, registers, and counters Design of synchronous sequential circuits Use of the basic building blocks in designing larger systems It also includes chapters that deal with important, but more advanced topics: Design of asynchronous sequential circuits Testing of logic circuits For students who have had no exposure to basic electronics, but are interested in learning a few key concepts, there is a chapter that presents the most basic aspects of electronic implementation of digital circuits. Major changes in the second edition of the book include new examples to clarify the presentation of fundamental concepts over 50 new examples of solved problems provided at the end of chapters NAND and NOR gates now introduced in Chapter 2 more complete discussion of techniques for minimization of logic functions in Chapter 4 (including the tabular method) a new chapter explaining the CAD flow for synthesis of logic circuits Altera's Quartus II CAD software provided on a CD-ROM three appendices that give tutorials on the use of Quartus II software

This book is intended for the graduate or advanced undergraduate engineer. The primary motivation for writing the text was to present a complete tutorial of phase-locked loops with a consistent notation. As such, it can serve as a textbook in formal classroom instruction, or as a self-study guide for the practicing engineer. A former colleague, Kevin Kreitzer, had suggested that I write a text, with an emphasis on digital phase-locked loops. As modem designers, we were continually receiving requests from other engineers asking for a definitive reference on digital phase-locked loops. There are several good papers in the literature, but there was not a good textbook for either classroom or self-paced study. From my own experience in designing low phase noise synthesizers, I also knew that third-order analog loop design was omitted from most texts. With those requirements, the material in the text seemed to flow naturally. Chapter 1 is the early history of phase-locked loops. I believe that historical knowledge can provide insight to the development and progress of a field, and phase-locked loops are no exception. As discussed in Chapter 1, consumer electronics (color television) prompted a rapid growth in phase-locked loop theory and applications, much like the wireless communications growth today. xiv Preface Although all-analog phase-locked loops are becoming rare, the continuous time nature of analog loops allows a good introduction to phase-locked loop theory.

This exciting new book covers various types of digital phase lock loops. It presents a comprehensive coverage of a new class of digital phase lock loops called the time delay tanlock loop (TDTL). It also details a number of architectures that improve the performance of the TDTL through adaptive techniques that overcome the conflicting requirements of the locking rage and speed of acquisition.

A controller for an all digital phase locked loop which operates by pulse addition and removal is investigated. Being a first order system, the digital phase locked loop is more limited in regard to parameter controls than its second order analog counterpart. A loop with a fast lock time generally has poor phase/frequency accuracy, while a loop programmed for high accuracy will have slow lock time. Given that the digital phase locked loop is digitally programmable, a set of parameters may be selected which will minimize the lock time of the loop. Once the loop is locked, the parameters may be changed to alter the loop bandwidth and increase the loop accuracy. A controller circuit has been designed to adjust loop parameters in such a manner thereby optimizing loop performance. The exclusive-OR phase detector which is commonly used with the pulse addition/removal type digital phase locked loop has a phase lock range of plus or minus a quarter of a cycle. This work investigates the loop response to an incoming signal which is outside of the phase lock range of phase detector and inside the frequency lock range of the loop. A sub-circuit is proposed to improve the lock time of the loop when it encounters an incoming signal with these characteristics. The proposed circuits were designed using integrated circuit layout tools and submitted to a semiconductor manufacturer for fabrication. The controller concept and results of simulations and prototype experiments are presented.

Phase Locked Loops (PLLs) are electronic circuits used for frequency control. Anything using radio waves, from simple radios and cell phones to sophisticated military communications gear uses PLLs.The communications industry’s big move into wireless in the past two years has made this mature topic red hot again. The fifth edition of this classic circuit reference comes complete with extremely valuable PLL design software written by Dr. Best. The software alone is worth many times the price of the book. The new edition also includes new chapters on frequency synthesis, CAD for PLLs, mixed-signal PLLs, and a completely new collection of sample communications applications.

This book describes the digitally intensive time-domain architectures and techniques applied to millimeter-wave frequency synthesis, with the objective of improving performance and reducing the cost of implementation. Coverage includes system architecture, system level modeling, critical building block design, and digital calibration techniques, making it highly suitable for those who want to learn about mm-wave frequency generation for communication and radar applications, integrated circuit implementation, and time-domain circuit and system techniques.

Highlights the challenges of frequency synthesis at mm-wave band using CMOS technology Compares the various approaches for mm-wave frequency generation (pros and cons) Introduces the digitally intensive synthesizer approach and its advantages Discusses the proper partitioning of the digitally intensive mm-wave frequency synthesizer into mm-wave, RF, analog, digital and software components Provides detailed design techniques from system level to circuit level Addresses system modeling, simulation techniques, design-for-test, and layout issues Demonstrates the use of time-domain techniques for high-performance mm-wave frequency synthesis

A greatly revised and expanded account of phaselocktechnology The Third Edition of this landmark book presents new developmentsin the field of phaselock loops, some of which have never beenpublished until now. Established concepts are reviewed criticallyand recommendations are offered for improved formulations. The workreflects the author's own research and many years of hands-onexperience with phaselock loops. Reflecting the myriad of phaselock loops that are now found inelectronic devices such as televisions, computers, radios, and cellphones, the book offers readers much new material, including: * Revised and expanded coverage of transfer functions * Two chapters on phase noise * Two chapters examining digital phaselock loops * A chapter on charge-pump phaselock loops * Expanded discussion of phase detectors and of oscillators * A chapter on anomalous phaselocking * A chapter on graphical aids, including Bode plots, root locusplots, and Nichols charts As in the previous editions, the focus of the book is on underlyingprinciples, which remain valid despite technological advances.Extensive references guide readers to additional information tohelp them explore particular topics in greater depth. Phaselock Techniques, Third Edition is intended for practicingengineers, researchers, and graduate students. This criticallyacclaimed book has been thoroughly updated with new information andexpanded for greater depth.

Phase-Locked Loops for Wireless Communications: Digitial, Analog and Optical Implementations, Second Edition presents a complete tutorial of phase-locked loops from analog implementations to digital and optical designs. The text establishes a thorough foundation of continuous-time analysis techniques and maintains a consistent notation as discrete-time and non-uniform sampling are presented. New to this edition is a complete treatment of charge pumps and the complementary sequential phase detector. Another important change is the increased use of MATLAB®, implemented to provide more familiar graphics and reader-derived phase-locked loop simulation. Frequency synthesizers and digital divider analysis/techniques have been added to this second edition. Perhaps most distinctive is the chapter on optical phase-locked loops that begins with sections discussing components such as lasers and photodetectors and finishing with homodyne and heterodyne loops. Starting with a historical overview, presenting analog, digital, and optical PLLs, discussing phase noise analysis, and including circuits/algorithms for data synchronization, this volume contains new techniques being used in this field. Highlights of the Second Edition: Development of phase-locked loops from analog to digital and optical, with consistent notation throughout; Expanded coverage of the loop filters used to design second and third order PLLs; Design examples on delay-locked loops used to synchronize circuits on CPUs and ASICS; New material on digital dividers that dominate a frequency synthesizer's noise floor. Techniques to analytically estimate the phase noise of a divider; Presentation of optical phase-locked loops with primers on the optical components and fundamentals of optical mixing; Section on automatic frequency control to provide frequency-locking of the lasers instead of phase-locking; Presentation of charge pumps, counters, and delay-locked loops. The Second Edition includes the essential topics needed by wireless, optics, and the traditional phase-locked loop specialists to design circuits and software algorithms. All of the material has been updated throughout the book.

Abstract: In this thesis a Full Digital Phase Locked Loop is designed and implemented in 0.13um technology node from TSMC. This full digital PLL is more advantageous than a traditional analog PLL because it eliminates the need for very fine analog voltage generated in a charge pump and it can be process independent. The focus of this thesis is to design and analyze a Digital Phase Locked Loop. This PLL has a lock range of 108MHz to 770MHz . A seven stage numerically controlled oscillator is implemented. Each inverter in the ring oscillator is driven by 21 tri-state inverters in parallel. To enable frequency control a 7 bit control word is decoded to enable these tri-state inverters. A second order integrating filter is used to average phase error and is clocked by control signals generated by a modified Phase Frequency Detector. This Full Digital PLL consumes 2.76mW of power when locked on at 720MHz.

Filling the gap in the market dedicated to PLL structures for power systems Internationally recognized expert Dr. Masoud Karimi-Ghartemani brings over twenty years of

experience working with PLL structures to Enhanced Phase-Locked Loop Structures for Power and Energy Applications, the only book on the market specifically dedicated to PLL architectures as they apply to power engineering. As technology has grown and spread to new devices, PLL has increased in significance for power systems and the devices that connect with the power grid. This book discusses the PLL structures that are directly applicable to power systems using simple language, making it easily digestible for a wide audience of engineers, technicians, and graduate students. Enhanced phase-locked loop (EPLL) has become the most widely utilized architecture over the past decade, and many books lack explanation of the structural differences between PLL and EPLL. This book discusses those differences and also provides detailed instructions on using EPLL for both single-phase applications and three-phase applications. The book’s major topics include: A basic look at PLL and its standard structure A full explanation of EPLL EPLL extensions and modifications Digital implementation of EPLL Extensions of EPLL to three-phase structures Dr. Karimi-Ghartemani provides basic analysis that helps readers understand each of the structures presented without requiring complicated mathematical proofs. His book is filled with illustrated examples and simulations that connect theory to the real world, making Enhanced Phase-Locked Loop Structures for Power and Energy Applications an ideal reference for anyone working with inverters, rectifiers, and related technologies.

Do you need to know how to develop more efficient digital communication systems? Based on the author's experience of over thirty years in industrial design, this practical guide provides detailed coverage of synchronization subsystems and their relationship with other system components. Readers will gain a comprehensive understanding of the techniques needed for the design, performance analysis and implementation of synchronization functions for a range of different modern communication technologies. Specific topics covered include frequency-looked loops in wireless receivers, optimal OFDM timing phase determination and implementation, and interpolation filter design and analysis in digital resamplers. Numerous implementation examples help readers to develop the necessary practical skills, and slides summarizing key concepts accompany the book online. This is an invaluable guide and essential reference for both practicing engineers and graduate students working in digital communications.

BURSTLOCK is a digital phase-locked loop implemented using Burst Processing. It is used in a receiver perform FM demodulation of commercial broadcast signals. It is also shown that BURSTLOCK has some theoretical advantages over conventional phase-locked loops. (Author).

This book presents a novel approach to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion. Readers will gain a deep understanding of ADPLLs and the central role played by noise-shaping. A range of ADPLL and TDC architectures are presented in unified manner. Analytical and simulation tools are discussed in detail. Matlab code is included that can be reused to design, simulate and analyze the ADPLL architectures that are presented in the book.

This modern, pedagogic textbook from leading author Behzad Razavi provides a comprehensive and rigorous introduction to CMOS PLL design, featuring intuitive presentation of theoretical concepts, extensive circuit simulations, over 200 worked examples, and 250 end-of-chapter problems. The perfect text for senior undergraduate and graduate students.

The book reports two approaches of implementation of the essential components of a Digital Phase Locked Loop based system for dealing with wireless channels showing Nakagami-m fading. It is mostly observed in mobile communication. In the first approach, the structure of a Digital phase locked loop (DPLL) based on Zero Crossing (ZC) algorithm is proposed. In a modified form, the structure of a DPLL based systems for dealing with Nakagami-m fading based on Least Square Polynomial Fitting Filter is proposed, which operates at moderate sampling frequencies. A sixth order Least Square Polynomial Fitting (LSPF) block and Roots Approximator (RA) for better phase-frequency detection has been implemented as a replacement of Phase Frequency Detector (PFD) and Loop Filter (LF) of a traditional DPLL, which has helped to attain optimum performance of DPLL. The results of simulation of the proposed DPLL with Nakagami-m fading and QPSK modulation is discussed in detail which shows that the proposed method provides better performance than existing systems of similar type.

The digital loop filter for an all-digital phase-locked loop was designed to meet a given set of specifications, and the performance of the filter was verified using MATLAB simulations. The number of bits used to represent each coefficients was selected so that the filter met specifications for magnitude while managing the are and power of the filter.